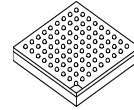


MC9328MXL

MC9328MXL



Package Information
Plastic Package
(MAPBGA–225 or 256)

Ordering Information

See [Table 2 on page 5](#)

1 Introduction

The i.MX Family of applications processors provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. The i.MX family specifically addresses the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The MC9328MXL (i.MXL) processor features the advanced and power-efficient ARM920T™ core that operates at speeds up to 200 MHz. Integrated modules, which include a USB device, an LCD controller, and an MMC/SD host controller, support a suite of peripherals to enhance portable products seeking to provide a rich multimedia experience. It is packaged in either a 256-contact Mold Array Process-Ball Grid Array (MAPBGA) or 225-contact MAPBGA package.

[Figure 1](#) shows the functional block diagram of the i.MXL processor.

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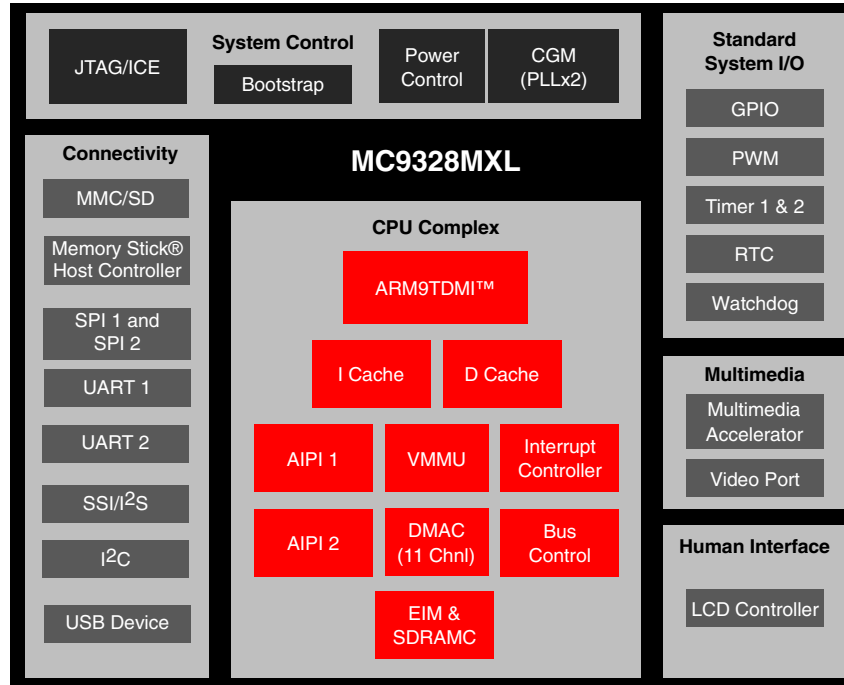


Figure 1. i.MXL Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Serial Peripheral Interface (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and an Inter-IC Sound (SSI/I²S) Module

- Inter-IC (I²C) Bus Module
- Video Port
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Multimedia Accelerator (MMA)
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 256-pin MAPBGA Package
- 225-contact MAPBGA Package

1.2 Target Applications

The i.MXL processor is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers, and messaging applications.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. i.MXL Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
256-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MXLVM20(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVM20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MXLVM15(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVM15(R2)
		-40°C to 85°C	Pb-free	MC9328MXLCVM15(R2)
225-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MXLVP20(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVP20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MXLVP15(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVP15(R2)
		-40°C to 85°C	Pb-free	MC9328MXLCVP15(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.

- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
 - *Active low* signals change from logic level one to logic level zero.
 - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
 - *Active low* signals change from logic level zero to logic level one.
 - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign (\$) or 0x are hexadecimal.

2 Signals and Connections

Table 2 identifies and describes the i.MXL processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. i.MXL Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
\overline{OE}	Memory Output Enable—Active low output enables external data bus.
\overline{CS} [5:0]	Chip-Select—The chip-select signals \overline{CS} [3:2] are multiplexed with \overline{CSD} [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default \overline{CSD} [1:0] is selected.
\overline{ECB}	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
\overline{LBA}	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK (burst clock)	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
\overline{RW}	\overline{RW} signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a \overline{WE} input signal by external DRAM.
\overline{DTACK}	\overline{DTACK} signal—The external input data acknowledge signal. When using the external \overline{DTACK} signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external \overline{DTACK} signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the i.MXL processor upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{CSD0}}$	SDRAM Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register.
$\overline{\text{CSD1}}$	SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
$\overline{\text{RAS}}$	SDRAM Row Address Select signal
$\overline{\text{CAS}}$	SDRAM Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
$\overline{\text{RESET_SF}}$	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
DMA	
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with \overline{ECB} , \overline{LBA} , BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SPI 1 and SPI 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SPI1_ \overline{SS}	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_ $\overline{SPI_RDY}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the <i>MC9328MXL Reference Manual</i> for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the <i>MC9328MXL Reference Manual</i> for information about how to bring this signal to the assigned pin.
SPI2_ \overline{SS}	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the <i>MC9328MXL Reference Manual</i> for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the <i>MC9328MXL Reference Manual</i> for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
USBD_ \overline{OE}	USB \overline{OE}
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1_RTS}}$	Request to Send
$\overline{\text{UART1_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2_RTS}}$	Request to Send
$\overline{\text{UART2_CTS}}$	Clear to Send
$\overline{\text{UART2_DSR}}$	Data Set Ready
$\overline{\text{UART2_RI}}$	Ring Indicator
$\overline{\text{UART2_DCD}}$	Data Carrier Detect
$\overline{\text{UART2_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I²S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I²C	
I2C_SCL	I ² C Clock
I2C_SDA	I ² C Data
PWM	
PWMO	PWM Output
Test Function	

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MXL processor.

3.1 Maximum Ratings

Table 3 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 4 on page 11 or the DC Characteristics table.

Table 3. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NVDD	DC I/O Supply Voltage	-0.3	3.3	V
QVDD	DC Internal (core = 150 MHz) Supply Voltage	-0.3	1.9	V
QVDD	DC Internal (core = 200 MHz) Supply Voltage	-0.3	2.0	V
AVDD	DC Analog Supply Voltage	-0.3	3.3	V
BTRFVDD	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800 ¹	1300 ²	mW

¹ A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core—that is, 7x GPIO, 15x Data bus, and 8x Address bus.

² A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core—that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 200MHz, and where the whole image is running out of SDRAM. QVDD at 2.0V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges for the supply voltages and temperatures. The i.MXL processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 5.

Table 4. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T _A	Operating temperature range MC9328MXLVM20/MC9328MXLVM15 MC9328MXLVP20/MC9328MXLVP15	0	70	°C
T _A	Operating temperature range MC9328MXLDVM20/MC9328MXLDVM15 MC9328MXLDVP20/MC9328MXLDVP15	-30	70	°C
T _A	Operating temperature range MC9328MXLCVM15/ MC9328MXLCVP15	-40	85	°C
NVDD	I/O supply voltage (if using MSHC, CSI, SPI, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 150 MHz)	1.70	1.90	V
QVDD	Internal supply voltage (Core = 200 MHz)	1.80	2.00	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the "Power-Up Sequence" section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 5 contains both maximum and minimum DC characteristics of the i.MXL processor.

Table 5. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
I _{op}	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
Sidd ₁	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	μA
Sidd ₂	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	μA
Sidd ₃	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	–	35	–	μA
Sidd ₄	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 55°C)	–	60	–	μA
V _{IH}	Input high voltage	0.7V _{DD}	–	V _{DD} +0.2	V
V _{IL}	Input low voltage	–	–	0.4	V
V _{OH}	Output high voltage (I _{OH} = 2.0 mA)	0.7V _{DD}	–	V _{DD}	V
V _{OL}	Output low voltage (I _{OL} = -2.5 mA)	–	–	0.4	V
I _{IL}	Input low leakage current (V _{IN} = GND, no pull-up or pull-down)	–	–	±1	μA
I _{IH}	Input high leakage current (V _{IN} = V _{DD} , no pull-up or pull-down)	–	–	±1	μA
I _{OH}	Output high current (V _{OH} = 0.8V _{DD} , V _{DD} = 1.8V)	–	–	4.0	mA
I _{OL}	Output low current (V _{OL} = 0.4V, V _{DD} = 1.8V)	-4.0	–	–	mA
I _{OZ}	Output leakage current (V _{out} = V _{DD} , output is high impedance)	–	–	±5	μA
C _i	Input capacitance	–	–	5	pF
C _o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from V_{DD min} to V_{DD max} under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 6. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 7. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms
EXTAL16M input jitter (peak to peak) ¹	–	TBD	TBD	–
EXTAL16M startup time ¹	TBD	–	–	–

¹ The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXL.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in [Figure 2](#). See [Table 8](#) for the ETM9 timing parameters used in [Figure 2](#).

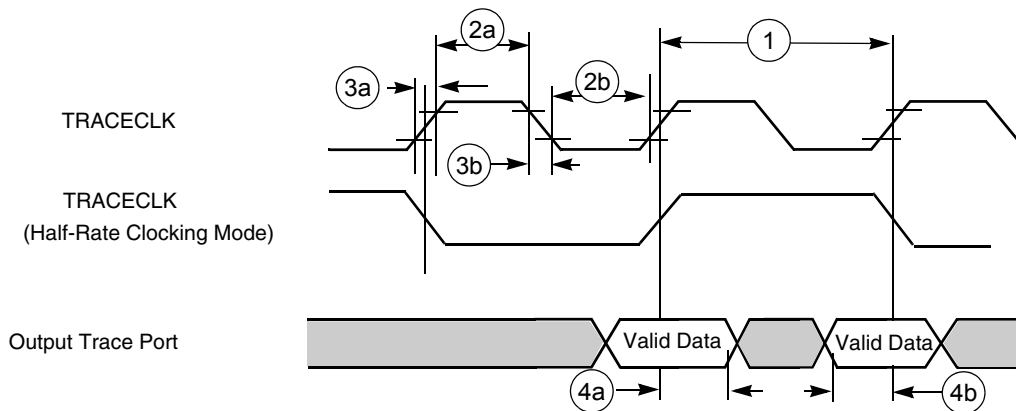


Figure 2. Trace Port Timing Diagram

Table 8. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 9. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 9. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock freq range	$V_{cc} = 1.8V$	5	–	100	MHz
Pre-divider output clock freq range	$V_{cc} = 1.8V$	5	–	30	MHz
Double clock freq range	$V_{cc} = 1.8V$	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–

Table 9. DPLL Specifications (Continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Pre-multiplier lock-in time	–	–	–	312.5	μsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 μs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 μs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 μs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 μs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \cdot T_{\text{dck}}$
Phase jitter (p-p)	Integer MF, FPL mode, $V_{\text{cc}}=1.8\text{V}$	–	1.0 (10%)	1.5	ns
Power supply voltage	–	1.7	–	2.5	V
Power dissipation	FOL mode, integer MF, $f_{\text{dck}} = 200 \text{ MHz}$, $V_{\text{cc}} = 1.8\text{V}$	–	–	4	mW

4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

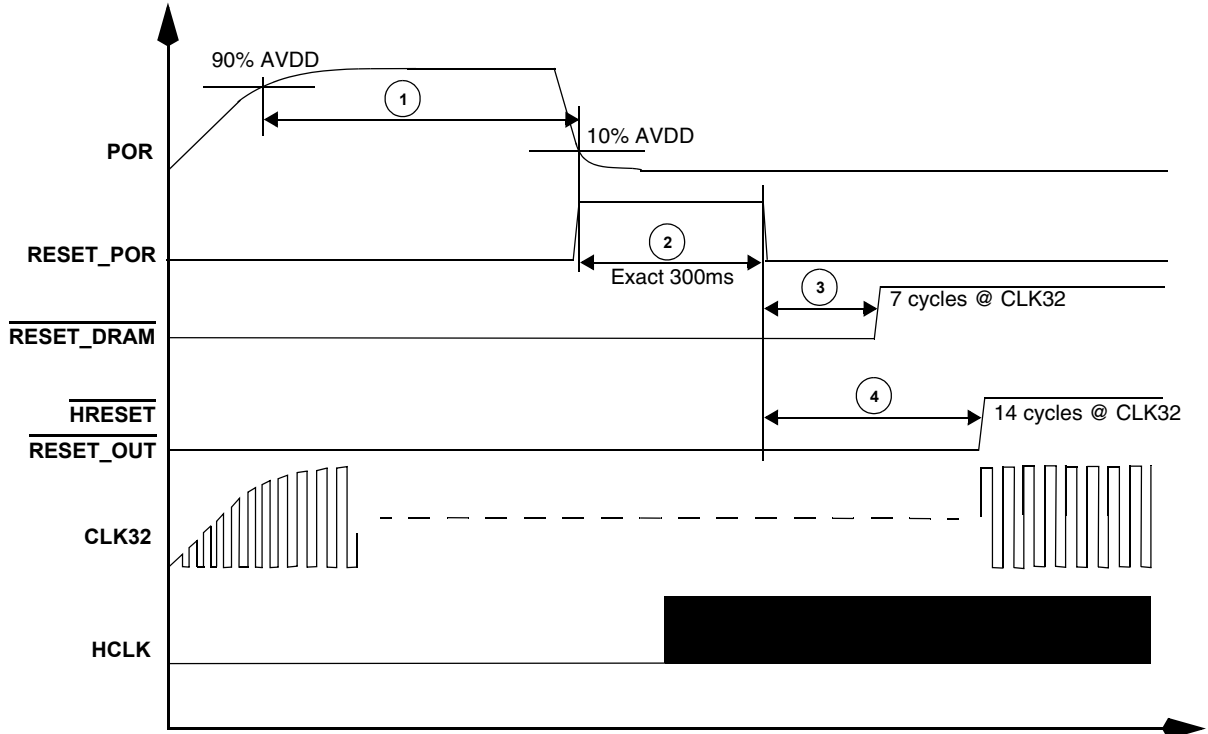


Figure 3. Timing Relationship with POR

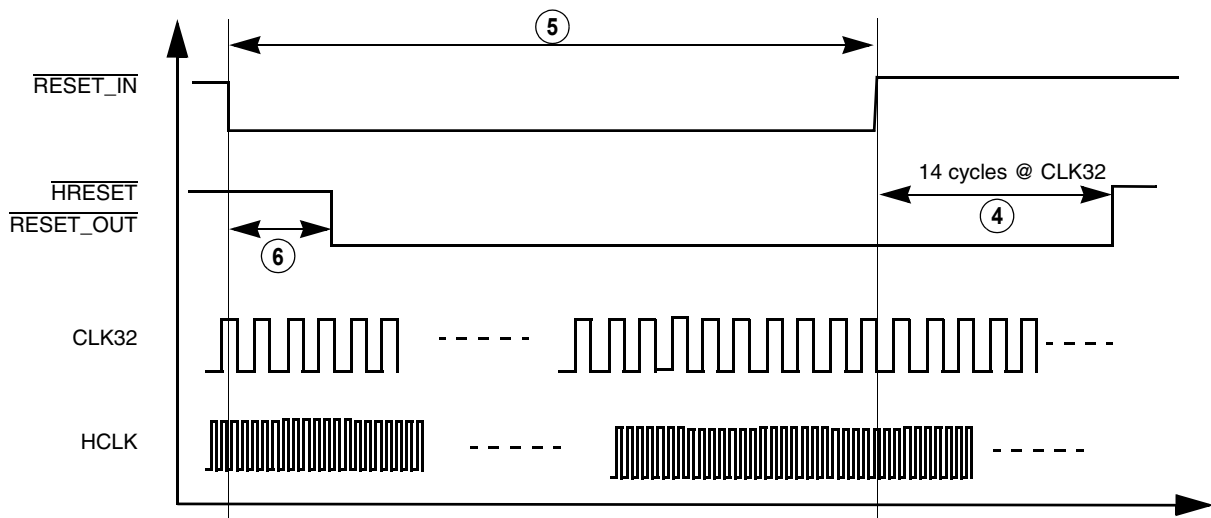


Figure 4. Timing Relationship with RESET_IN

Table 10. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	note ¹	–	note ¹	–	–
2	Width of internal POWER_ON_RESET (CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset HRESERT and output reset at pin RESET_OUT	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset RESET_IN	4	–	4	–	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

¹ POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal. If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MXL processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 11 defines the parameters of signals.

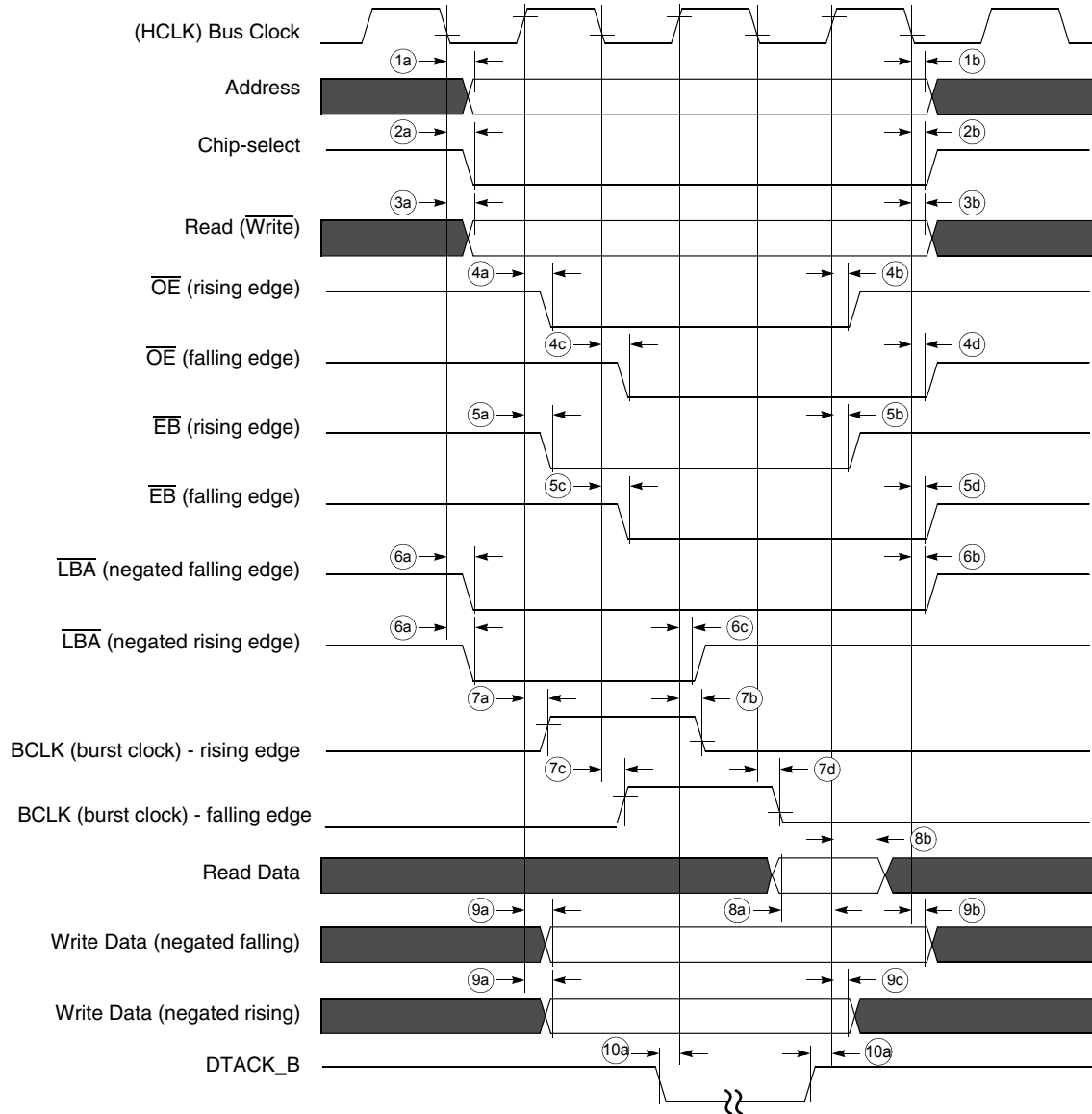


Figure 5. EIM Bus Timing Diagram

Table 11. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns

Table 11. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns
4a	Clock ¹ rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock ¹ rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock ¹ fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock ¹ fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock ¹ rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock ¹ rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock ¹ fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock ¹ fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock ¹ fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock ¹ fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock ¹ rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock ¹ rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock ¹ rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock ¹ fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock ¹ fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock ¹ rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock ¹ fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock ¹ rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

¹ Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports $\overline{\text{DTACK}}$ signal function when the external $\overline{\text{DTACK}}$ signal is used for data acknowledgement.

4.4.2 DTACK Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

4.4.2.1 WAIT Read Cycle without DMA

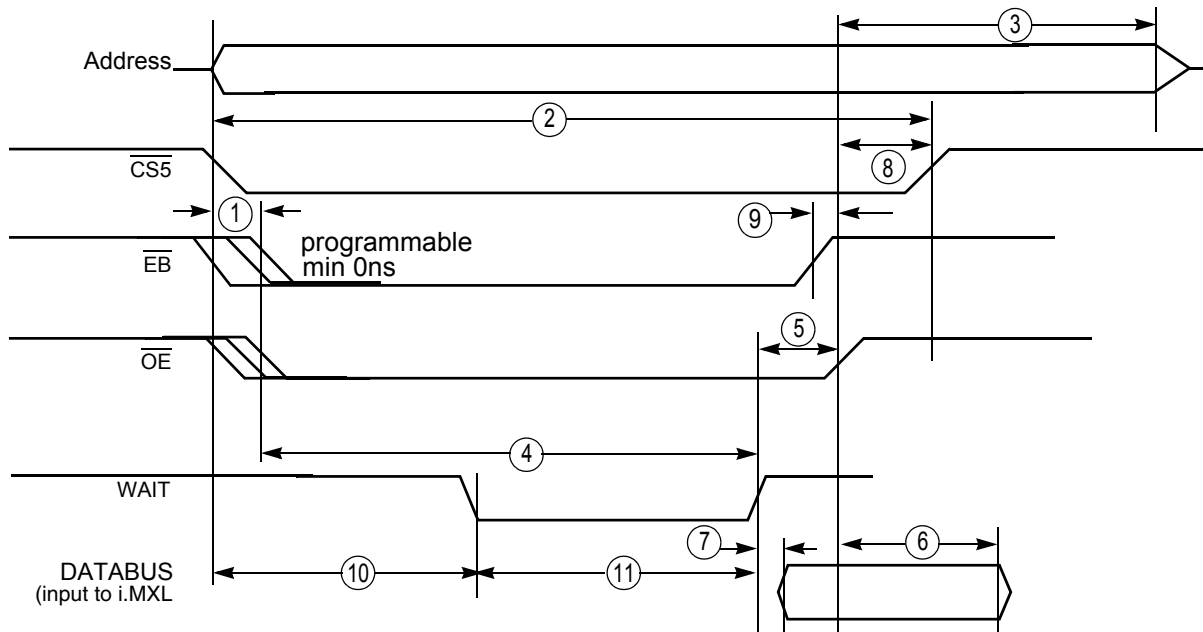


Figure 6. WAIT Read Cycle without DMA

Table 12. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	\overline{OE} and \overline{EB} assertion time	See note 2	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	\overline{OE} negated to address inactive	56.81	57.28	ns
4	Wait asserted after \overline{OE} asserted	–	1020T	ns
5	Wait asserted to \overline{OE} negated	2T+1.57	3T+7.33	ns
6	Data hold timing after \overline{OE} negated	T-1.49	–	ns
7	Data ready after wait asserted	0	T	ns
8	OE negated to CS negated	1.5T-0.68	1.5T-0.06	ns
9	OE negated after EB negated	0.06	0.18	ns
10	Become low after CS5 asserted	0	1019T	ns

Table 12. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
11	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. \overline{OE} and \overline{EB} assertion time is programmable by OEA bit in CS5L register. \overline{EB} assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and CS asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

4.4.2.2 WAIT Read Cycle DMA Enabled

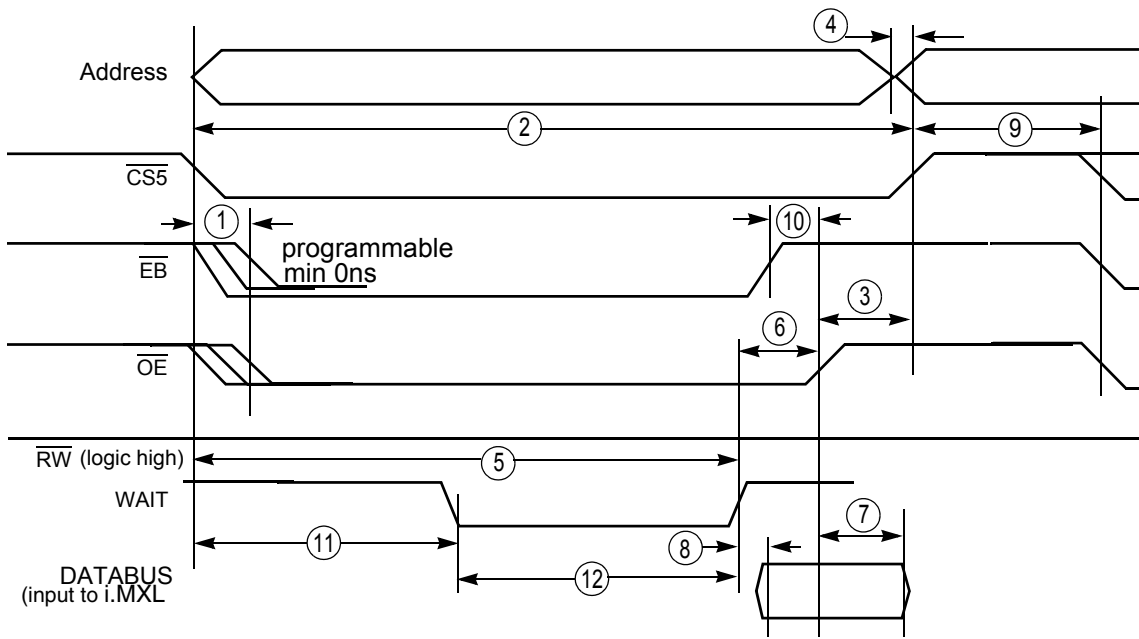


Figure 7. DTACK WAIT Read Cycle DMA Enabled

Table 13. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	\overline{OE} and \overline{EB} assertion time	See note 2	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	\overline{OE} negated before $\overline{CS5}$ is negated	1.5T-0.68	1.5T-0.06	ns
4	Address inactivated before $\overline{CS5}$ negated	–	0.05	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to \overline{OE} negated	2T+1.57	3T+7.33	ns

Table 13. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
7	Data hold timing after \overline{OE} negated	T-1.49	–	ns
8	Data ready after wait is asserted	–	T	ns
9	\overline{CS} deactive to next \overline{CS} active	T		ns
10	OE negate after EB negate	0.06	0.18	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. \overline{OE} and \overline{EB} assertion time is programmable by OEA bit in CS5L register. \overline{EB} assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and \overline{CS} asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

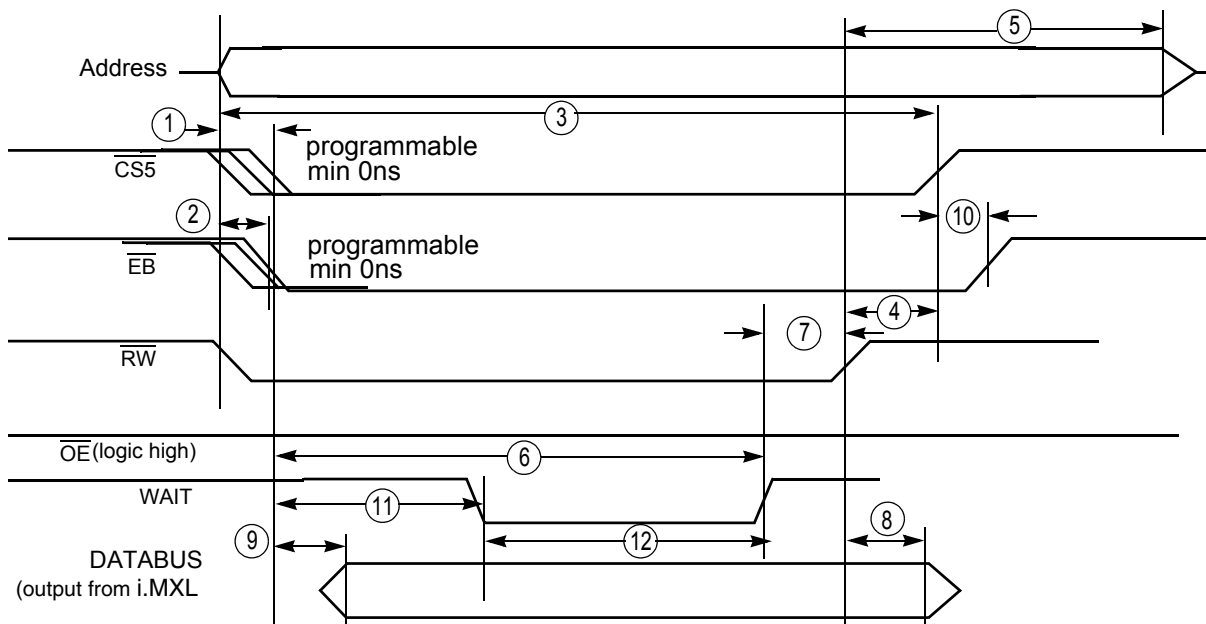


Figure 8. WAIT Write Cycle without DMA

Table 14. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	\overline{EB} assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	\overline{RW} negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	\overline{RW} negated to Address inactive	64.22	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to \overline{RW} negated	T+2.66	2T+7.96	ns
8	Data hold timing after \overline{RW} negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	\overline{EB} negated after $\overline{CS5}$ is negated	0.5T	0.5T+0.5	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. \overline{EB} assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and \overline{RW} asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.4 WAIT Write Cycle DMA Enabled

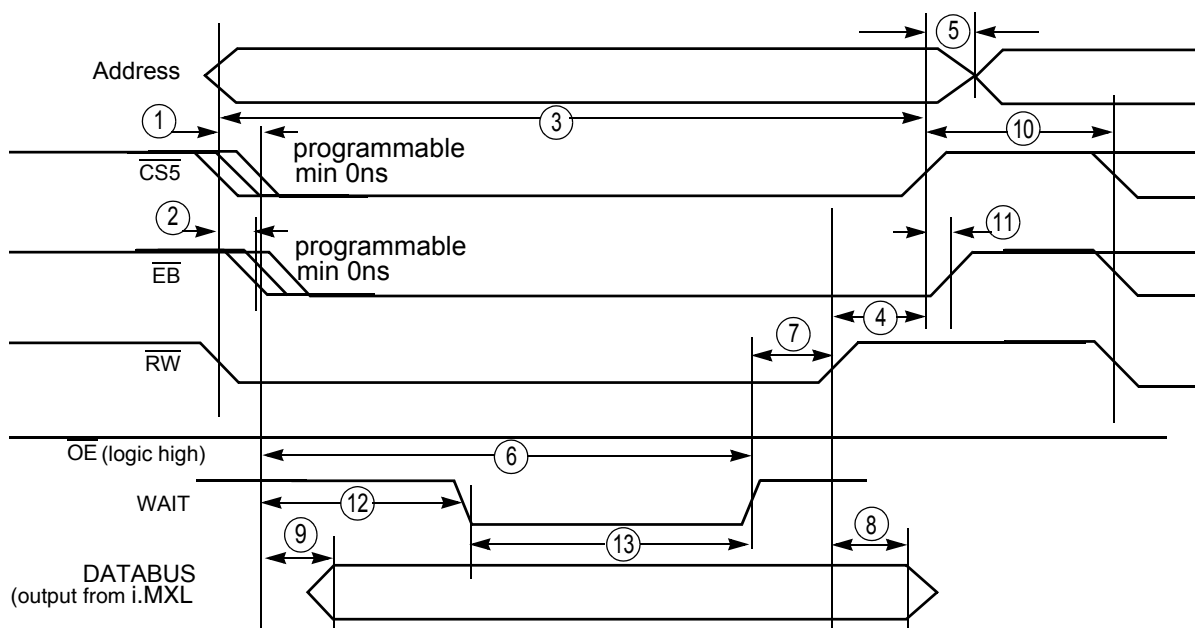


Figure 9. WAIT Write Cycle DMA Enabled

Table 15. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

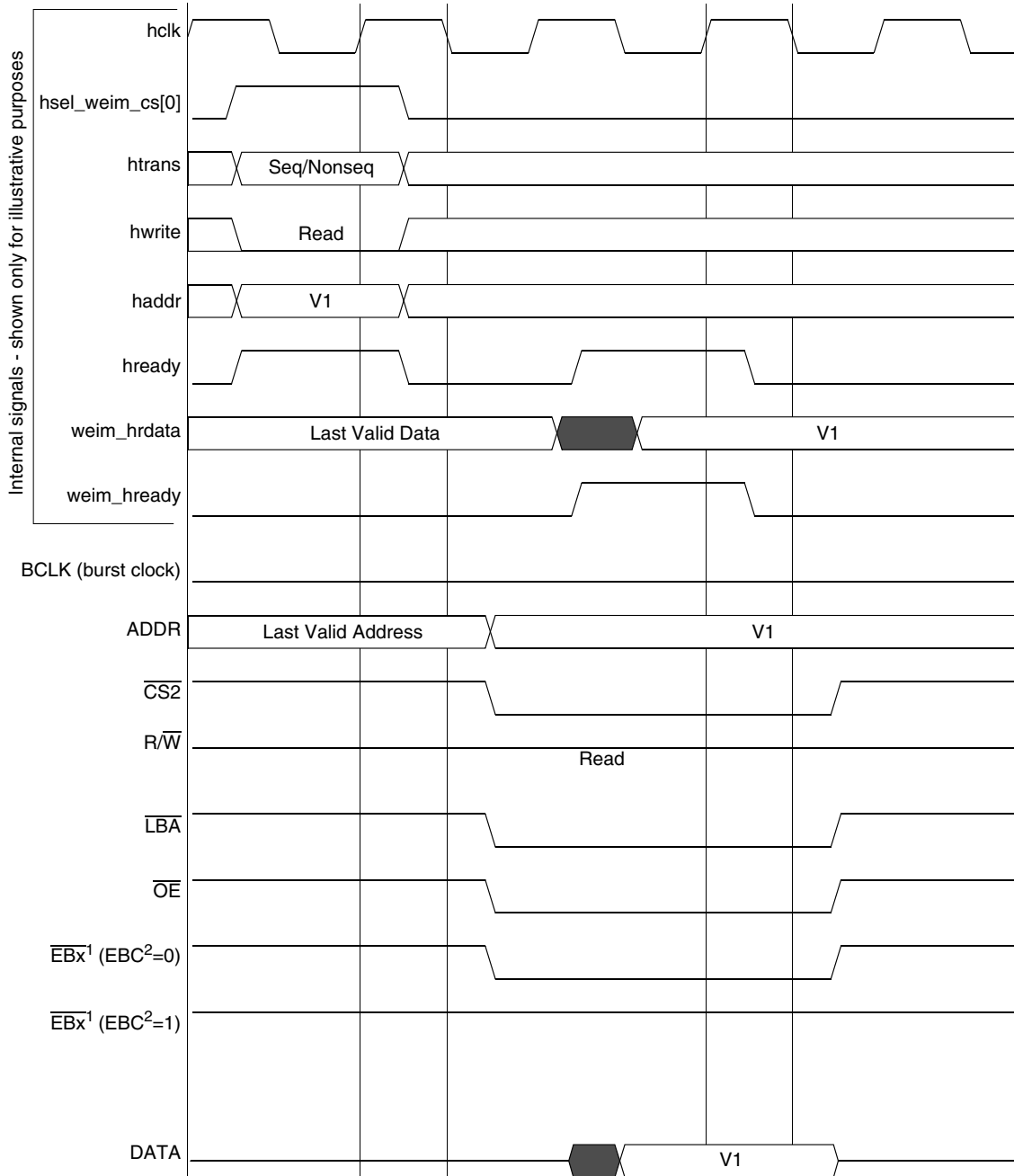
Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	\overline{EB} assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	\overline{RW} negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	Address inactivated after \overline{CS} negated	–	0.09	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to \overline{RW} negated	T+2.66	2T+7.96	ns
8	Data hold timing after \overline{RW} negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	\overline{CS} deactive to next \overline{CS} active	T	–	ns
11	\overline{EB} negate after \overline{CS} negate	0.5T	0.5T+0.5	
12	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. \overline{EB} assertion also can be programable by WEA bits in CS5L register.
3. Address becomes valid and \overline{RW} asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MXL, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 11 defines the parameters of signals.



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF

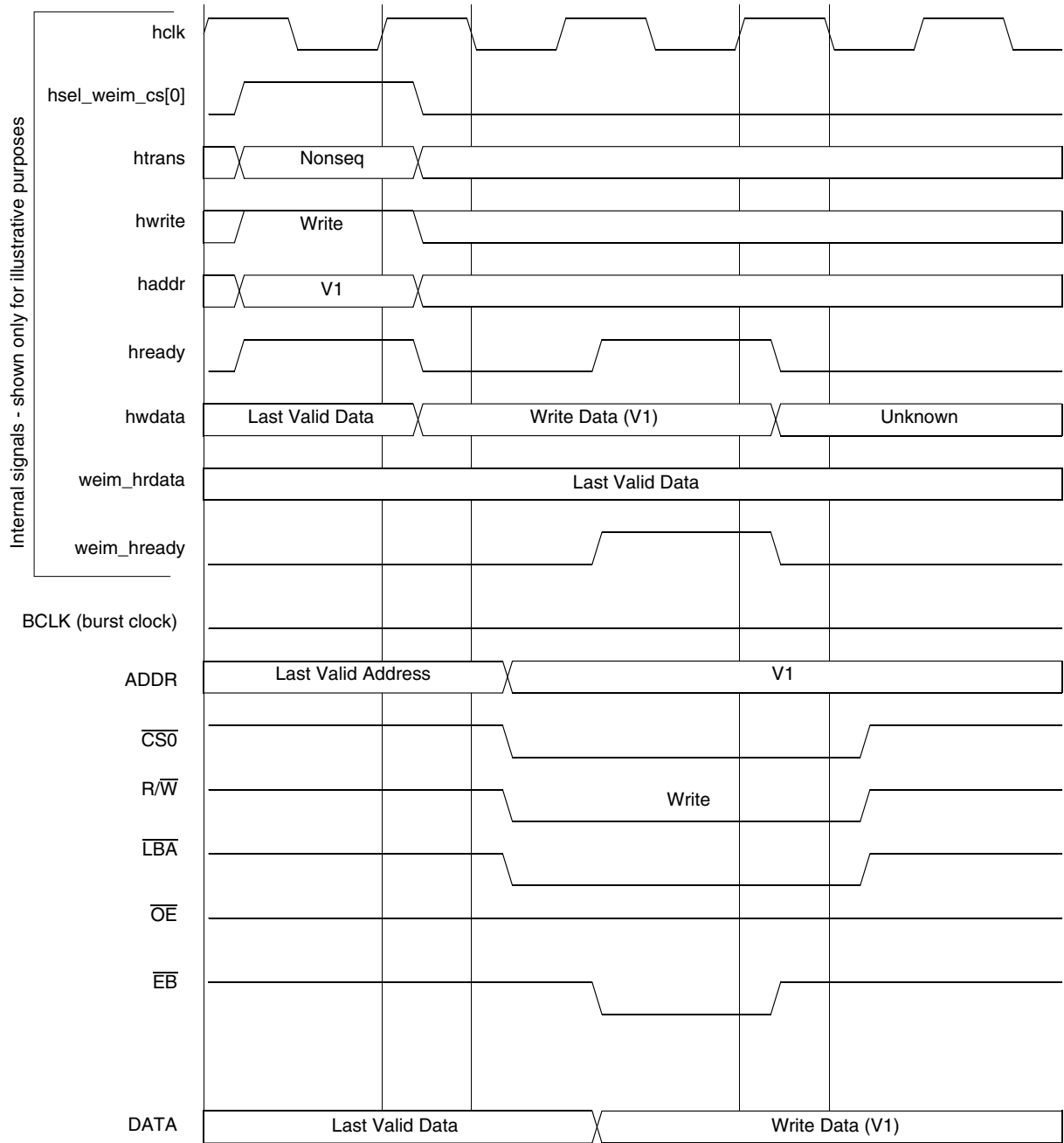
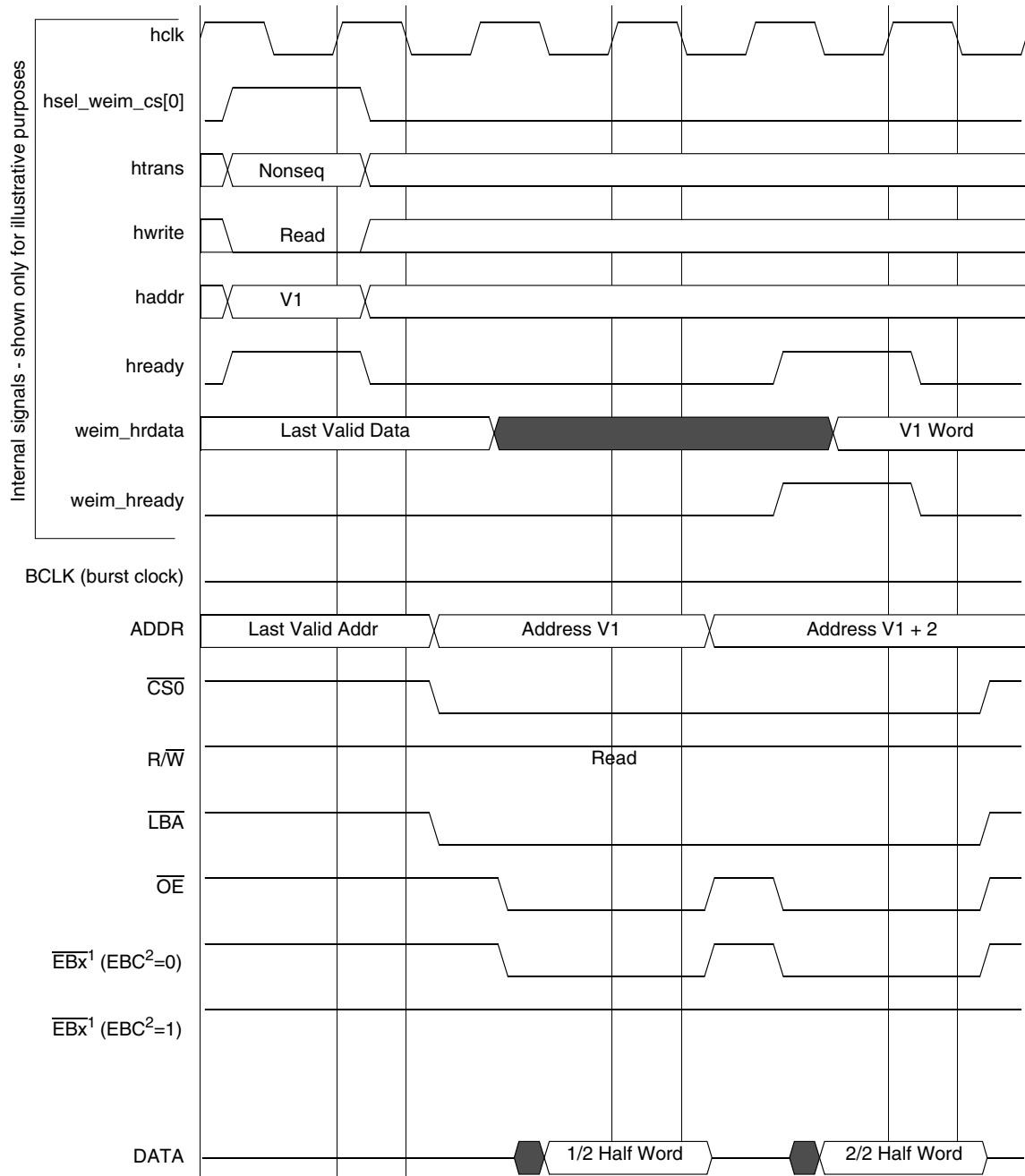


Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF

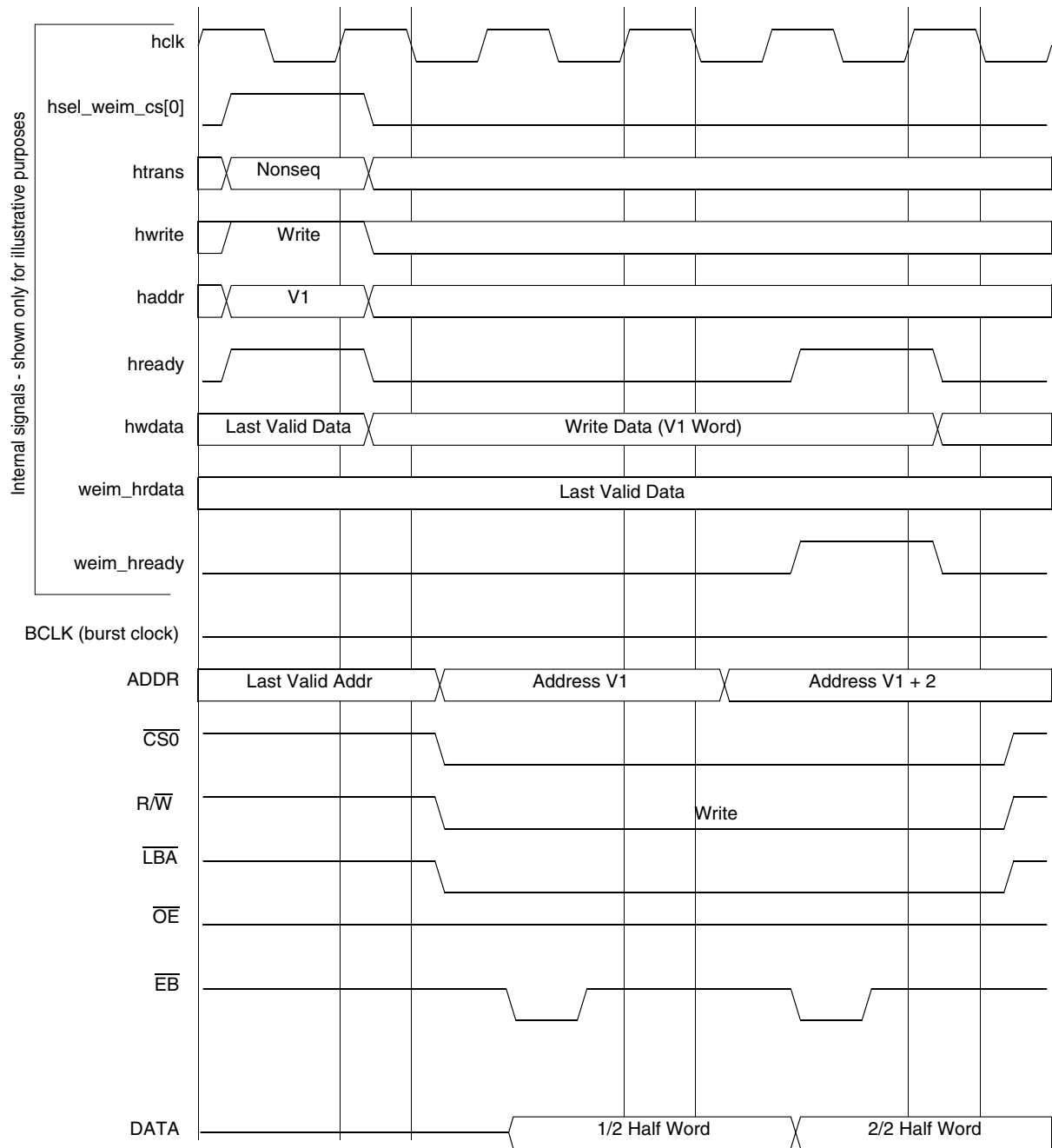
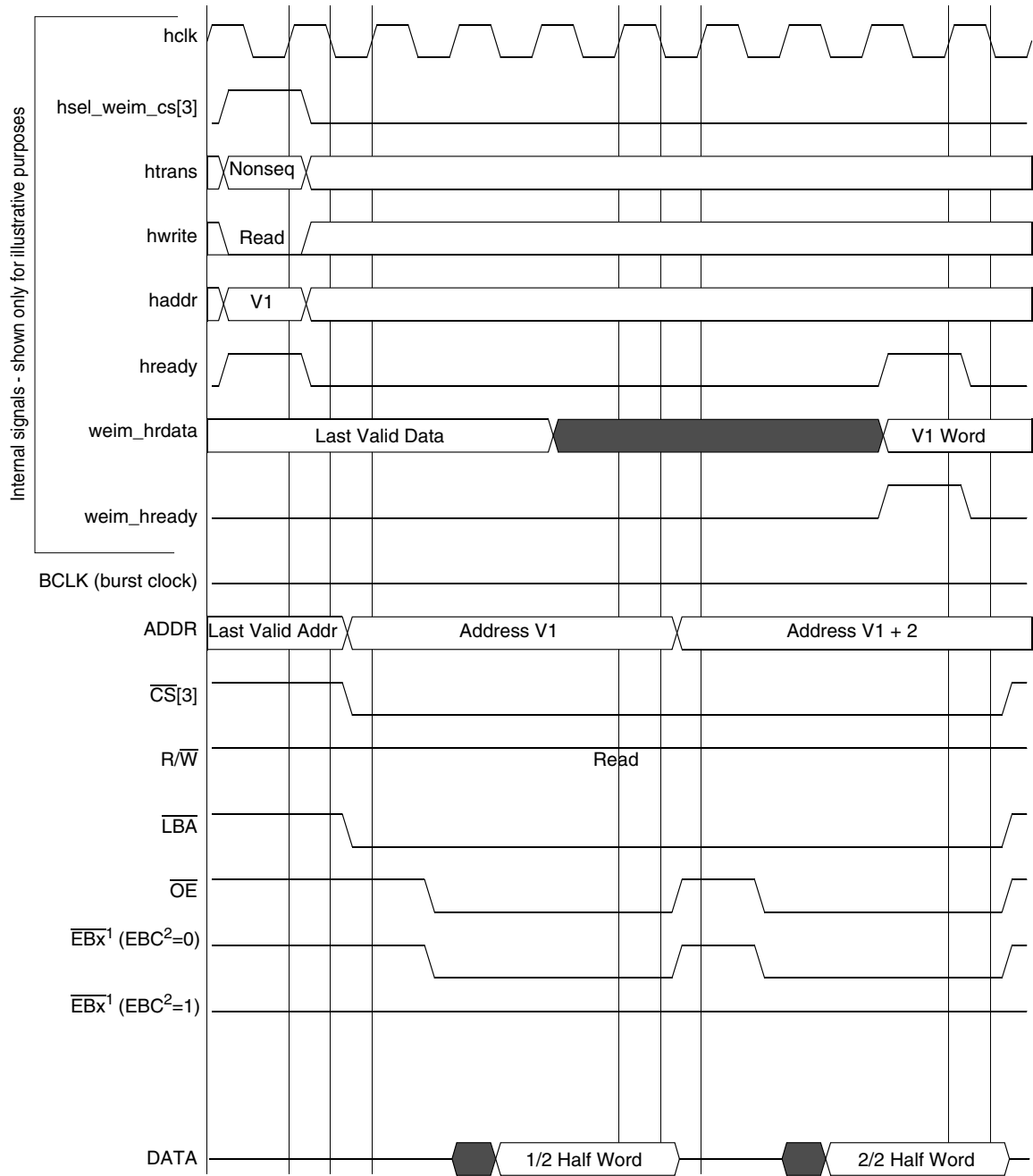


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF

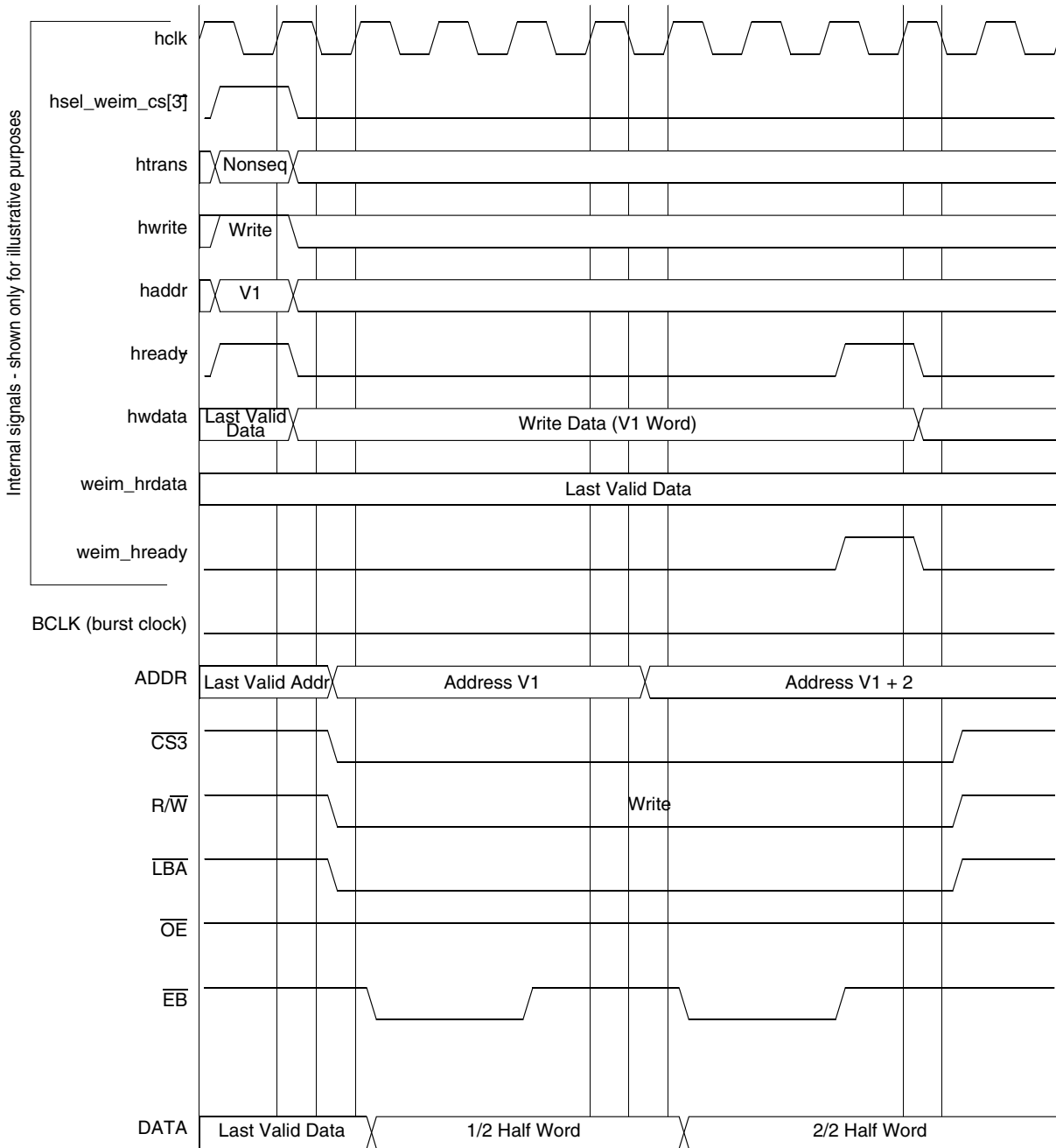
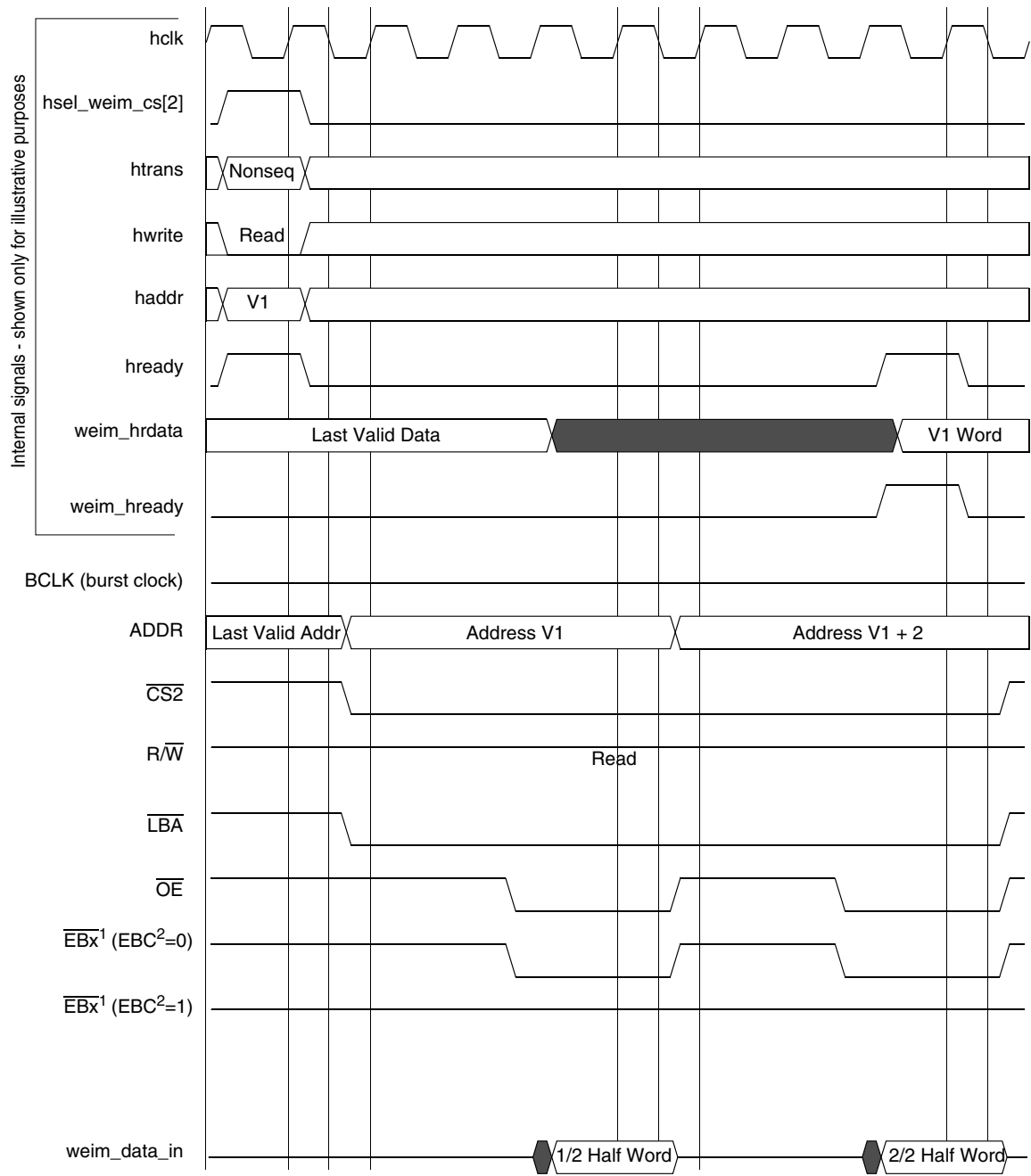


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF

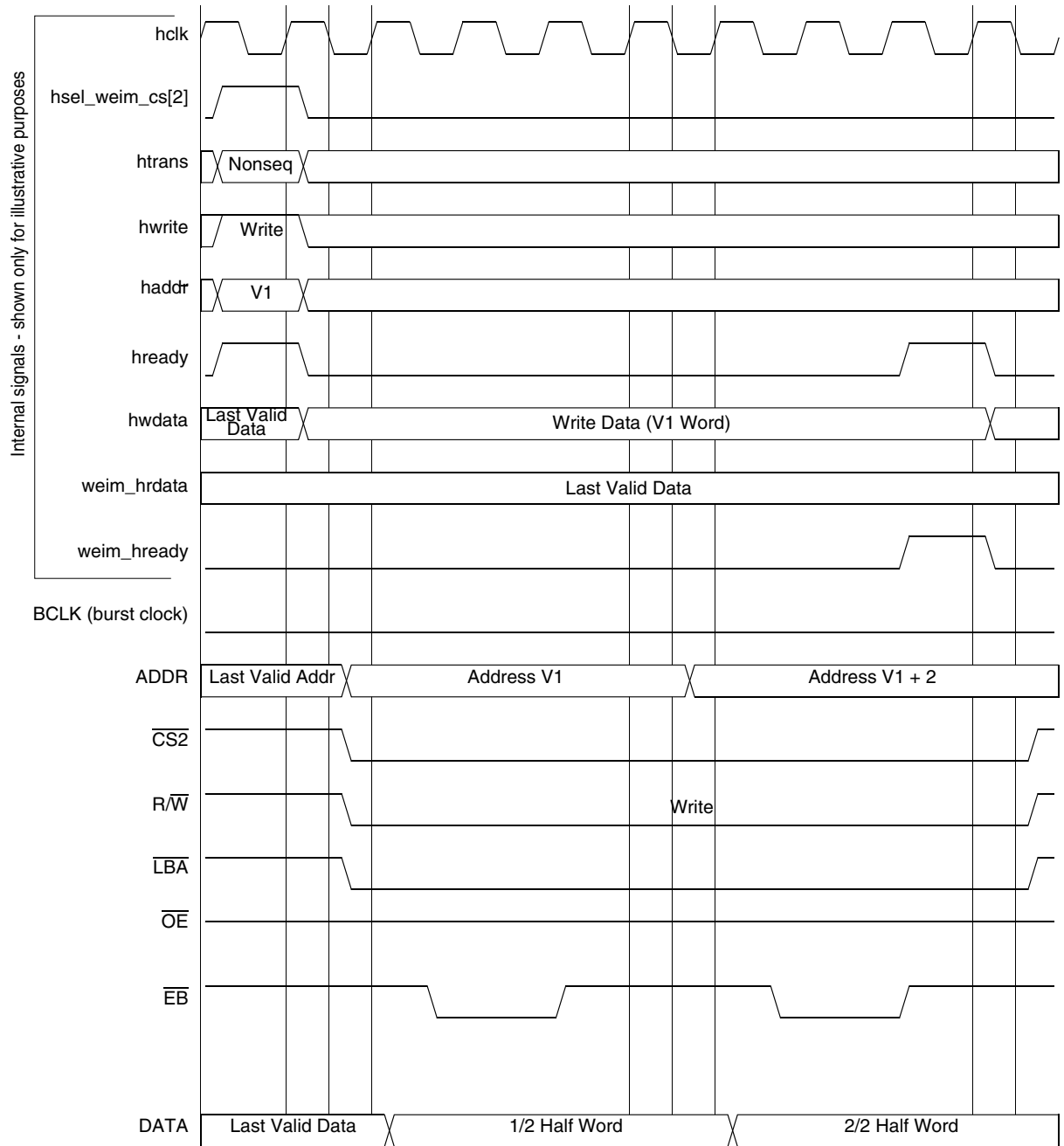
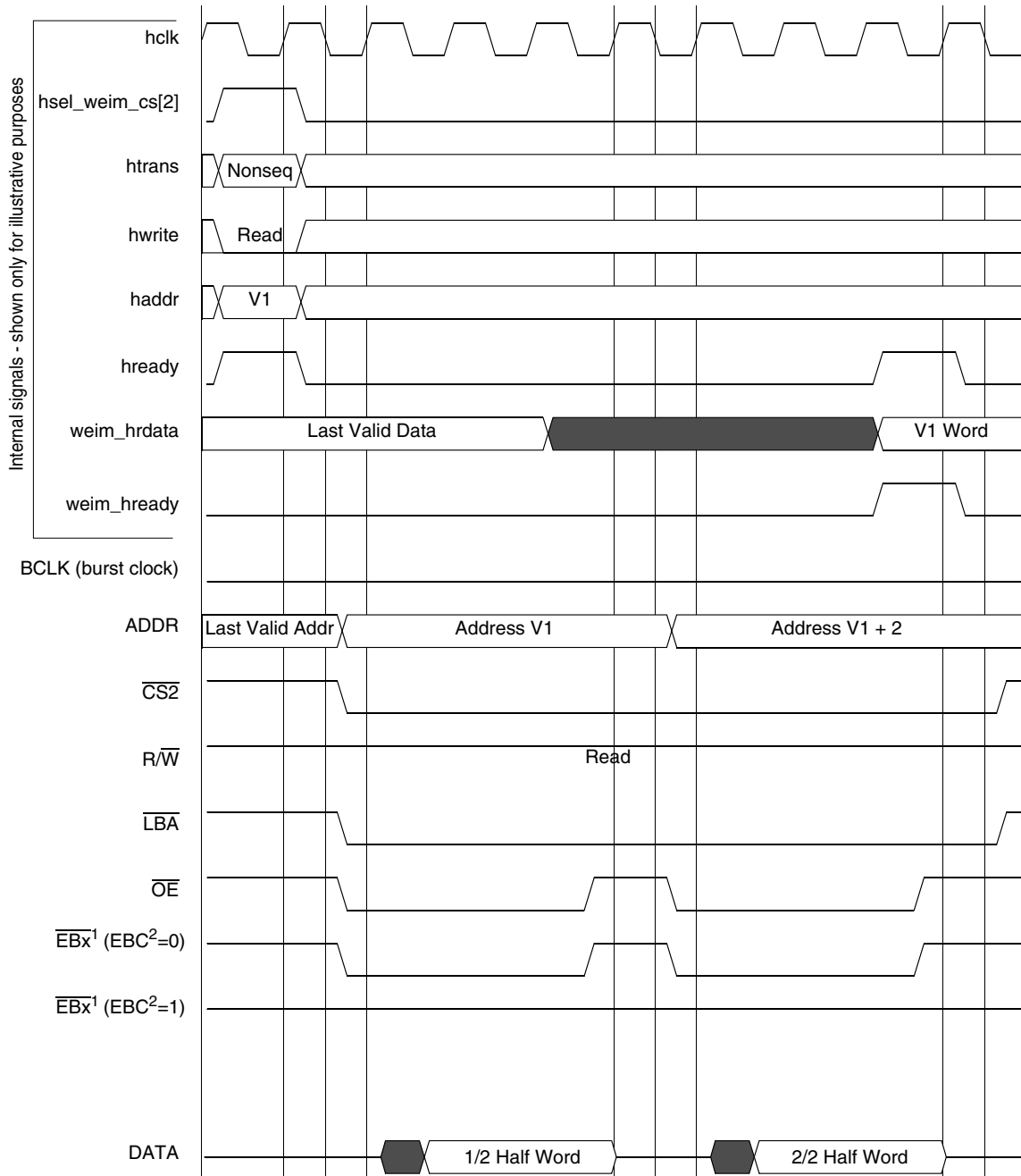


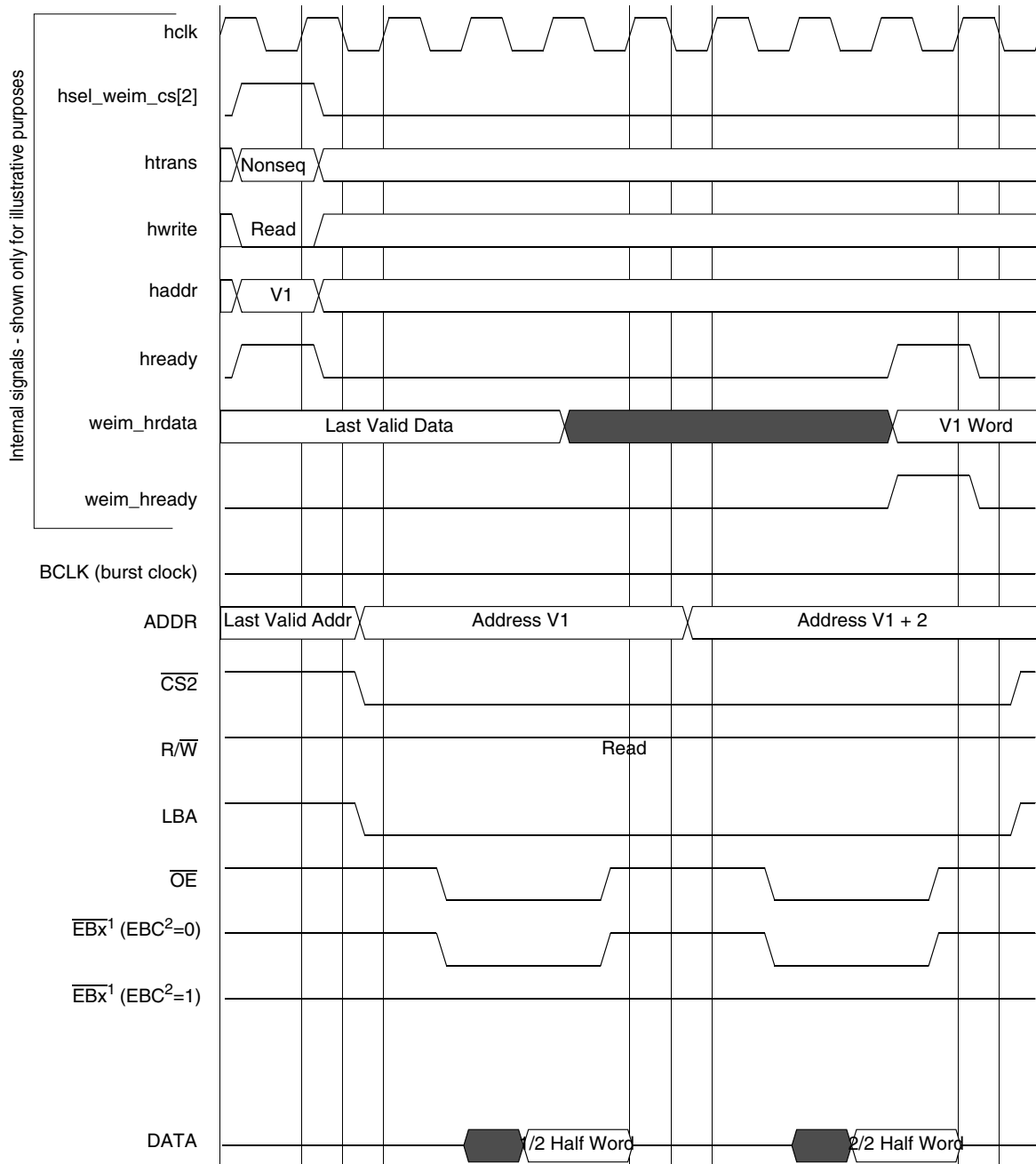
Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

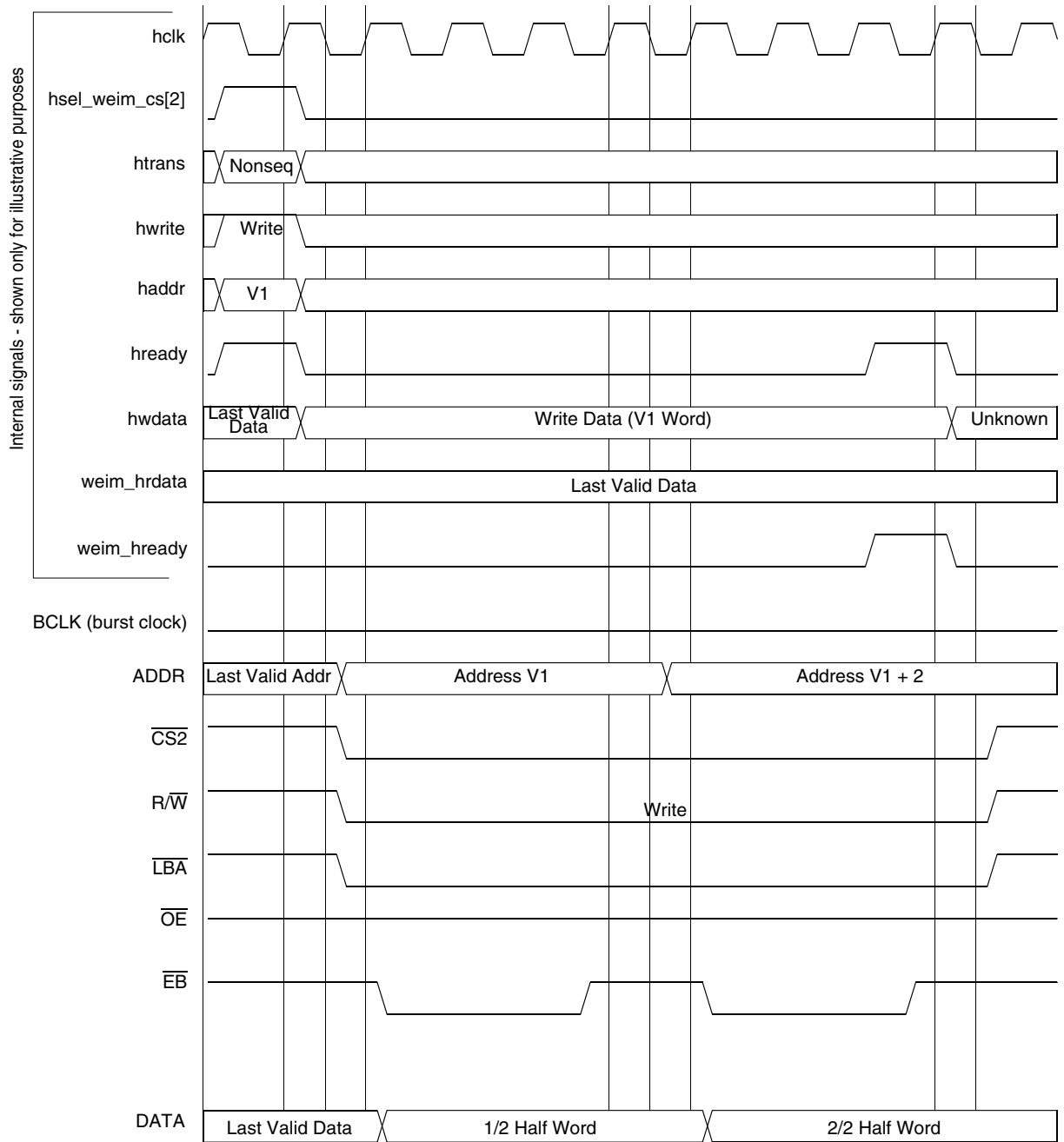


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

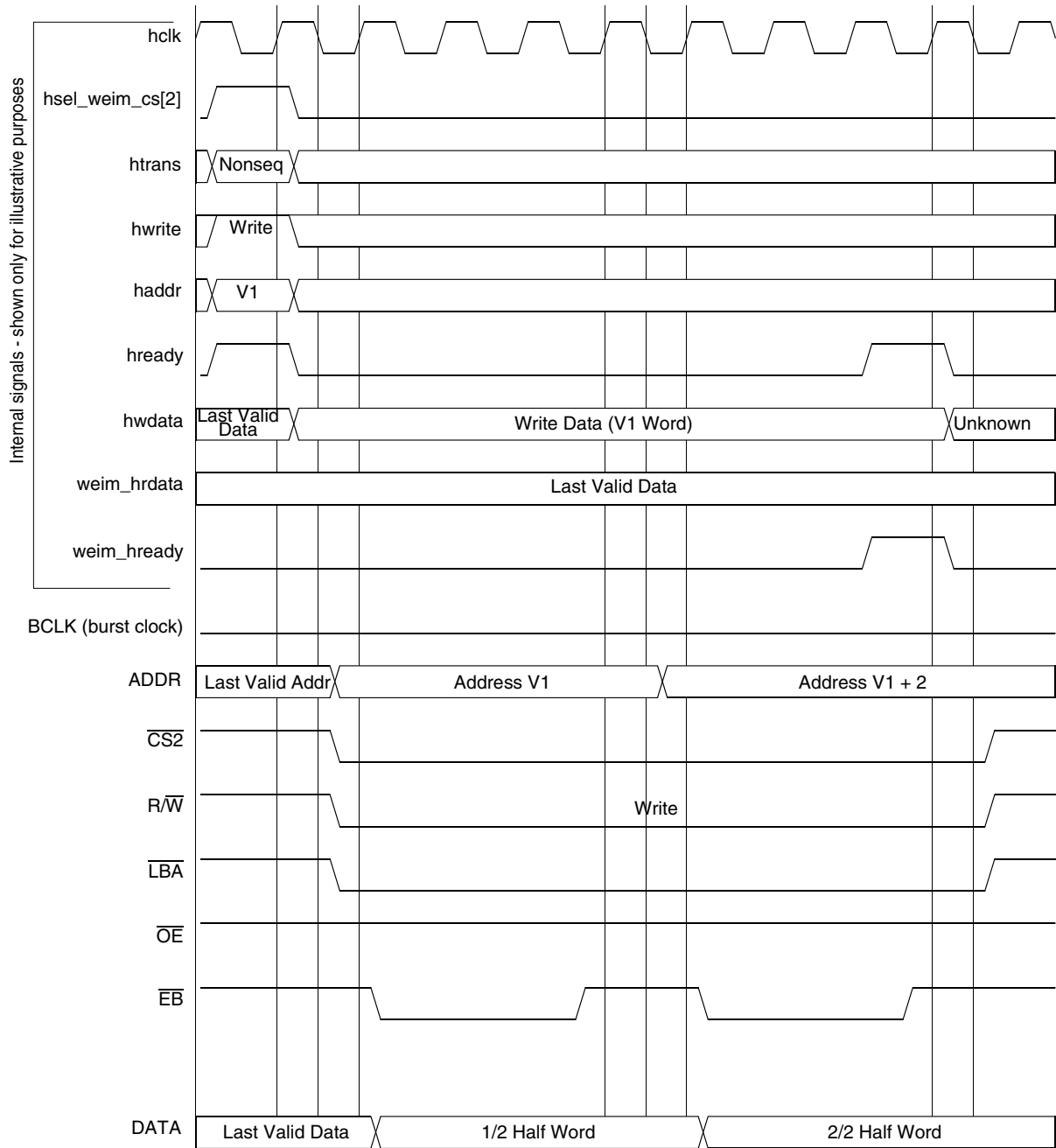
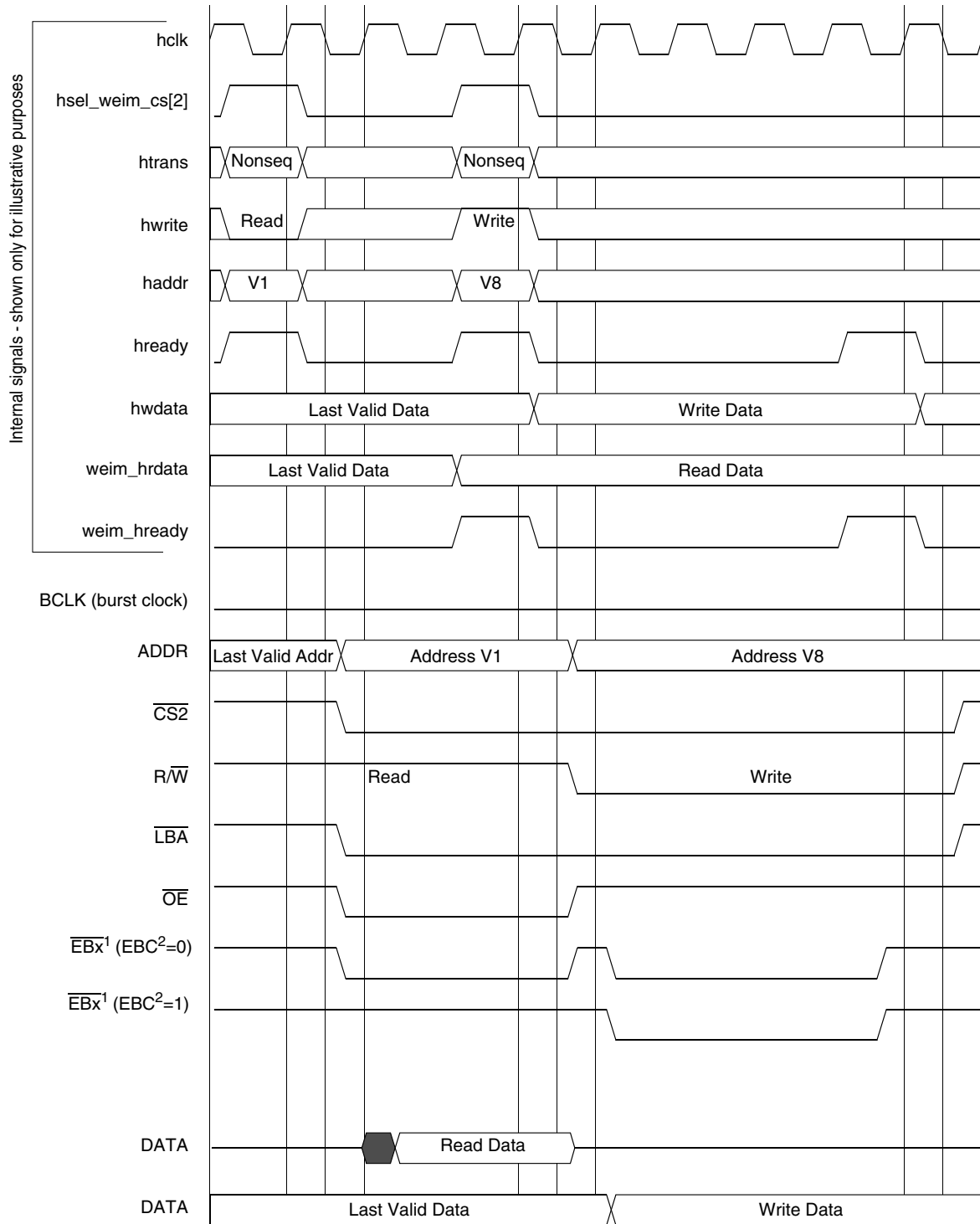


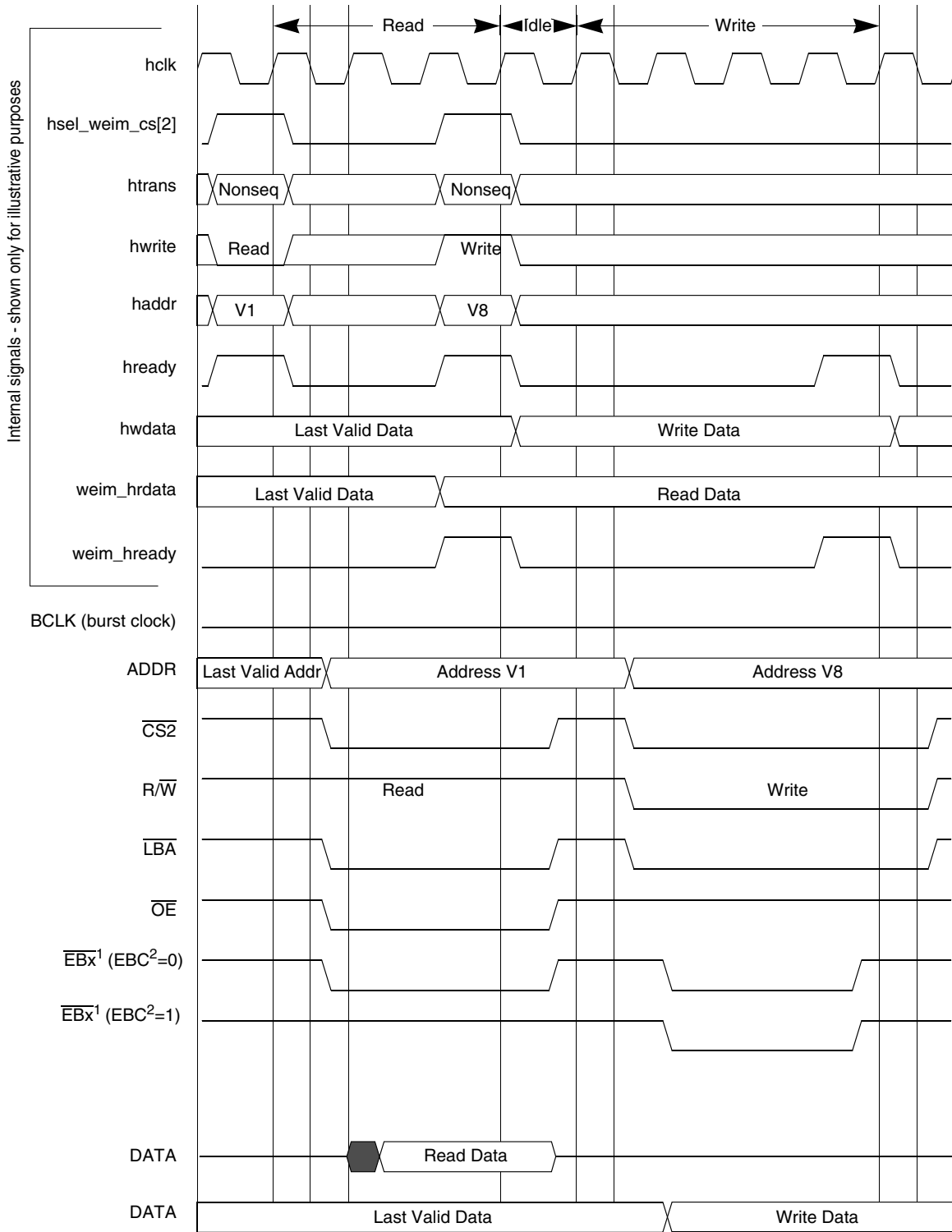
Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF

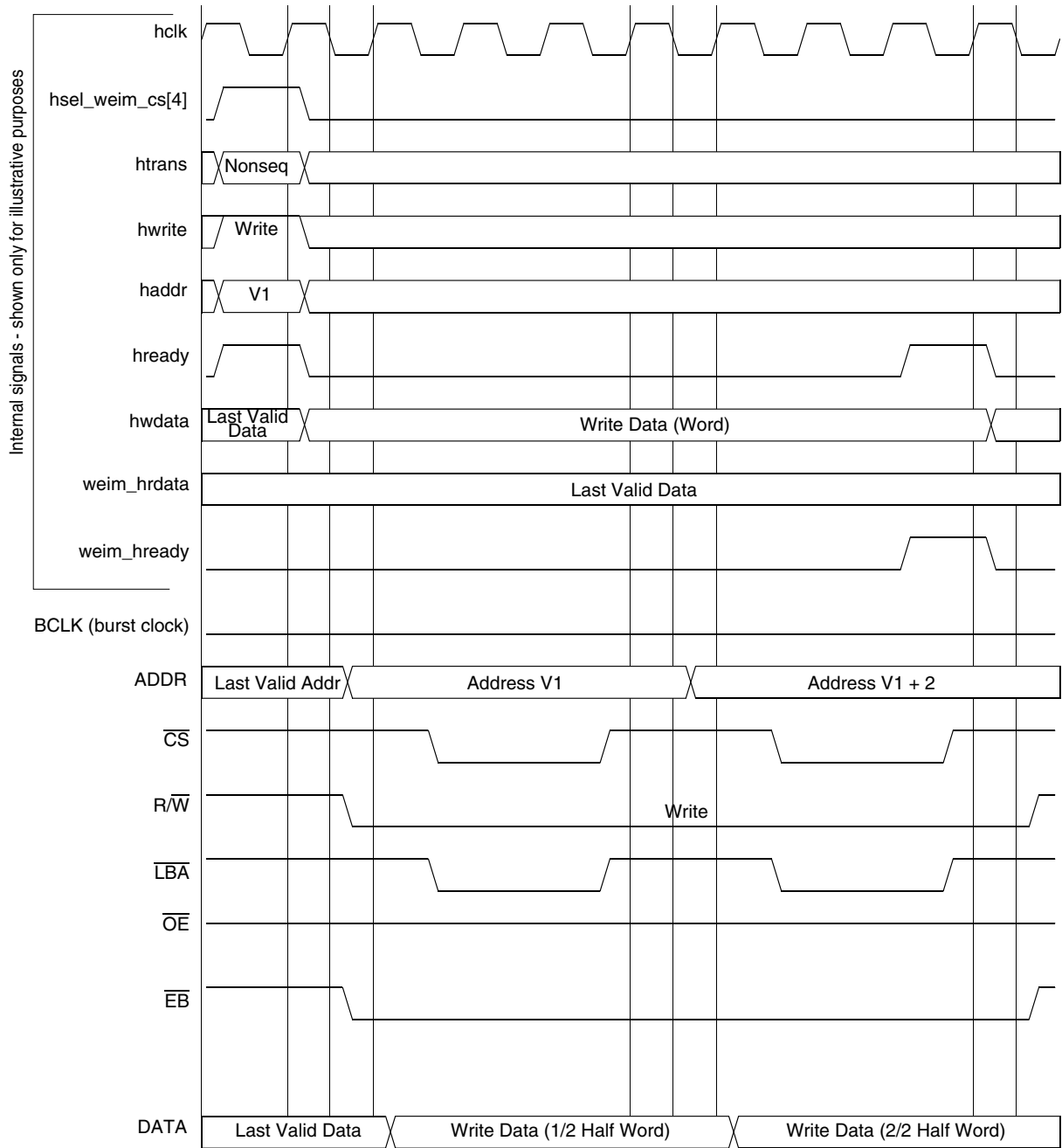
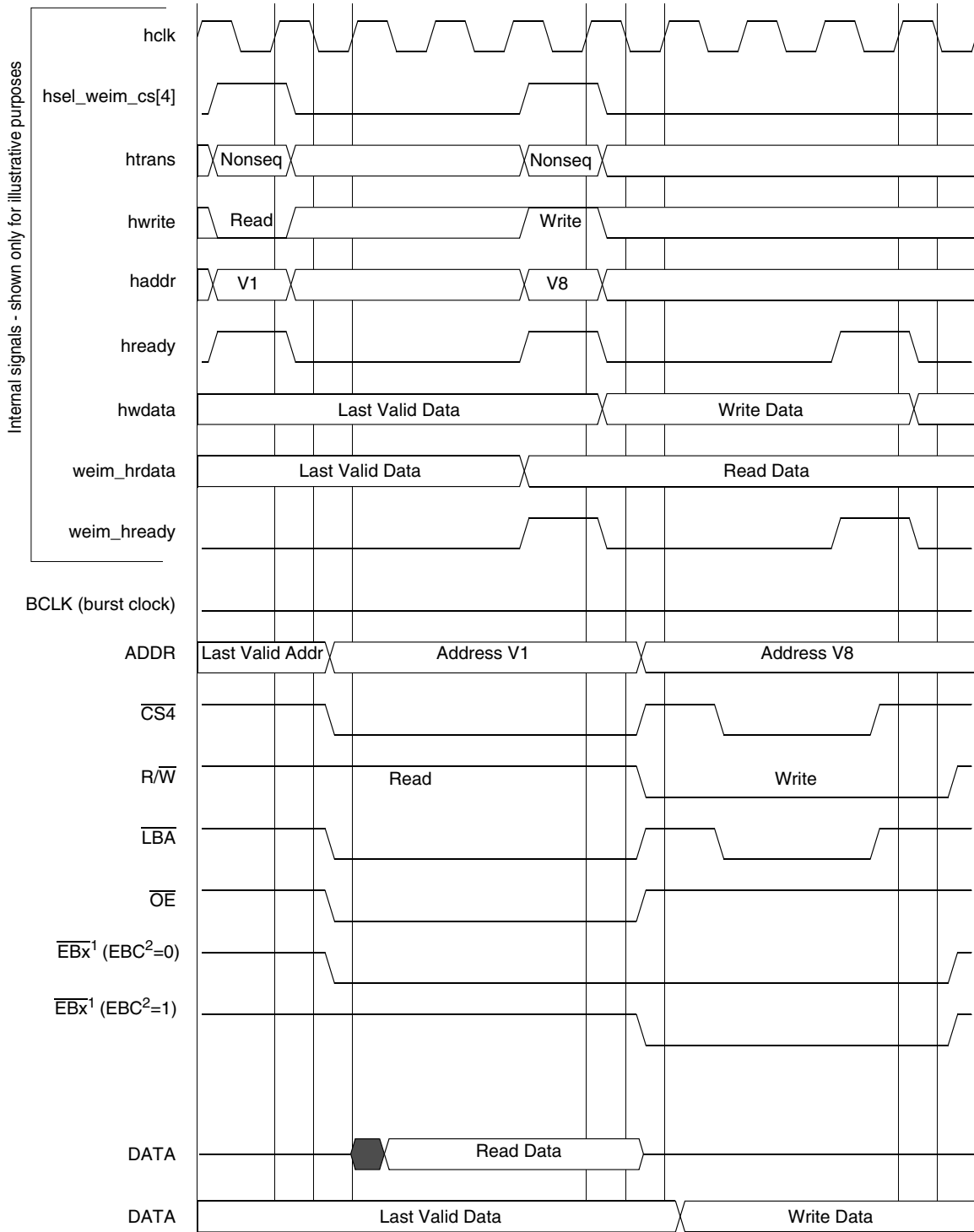
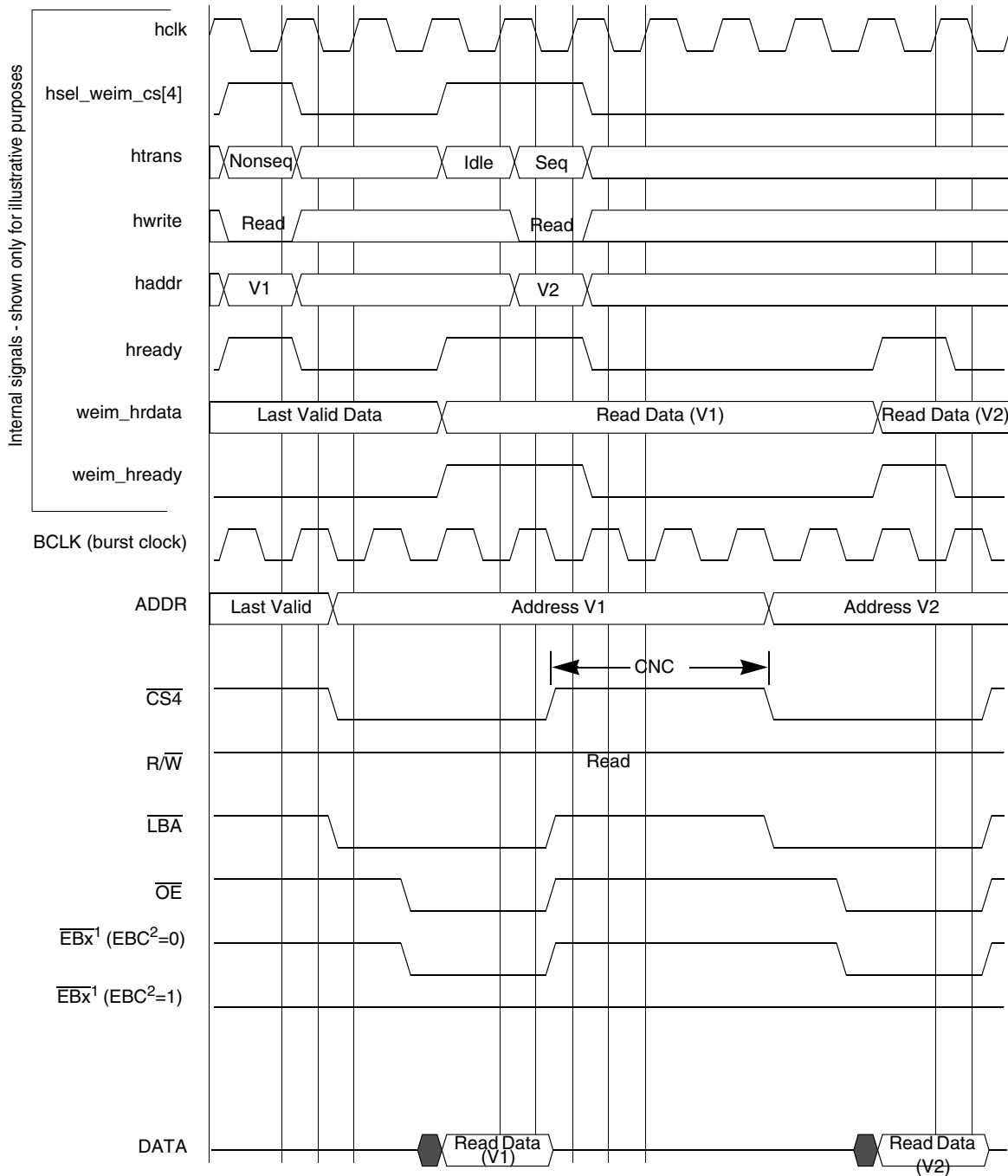


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

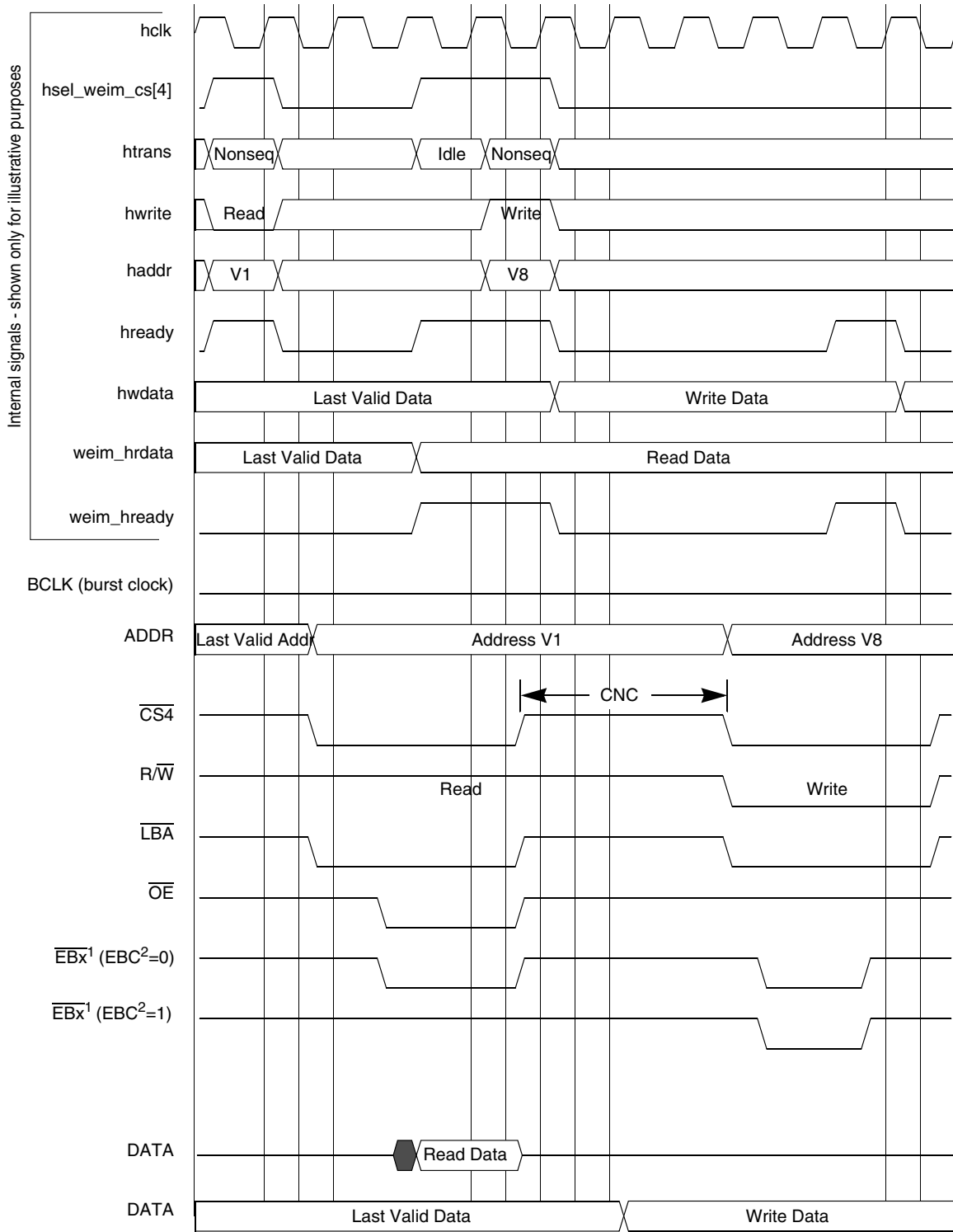
Figure 25. WSC = 3, CSA = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

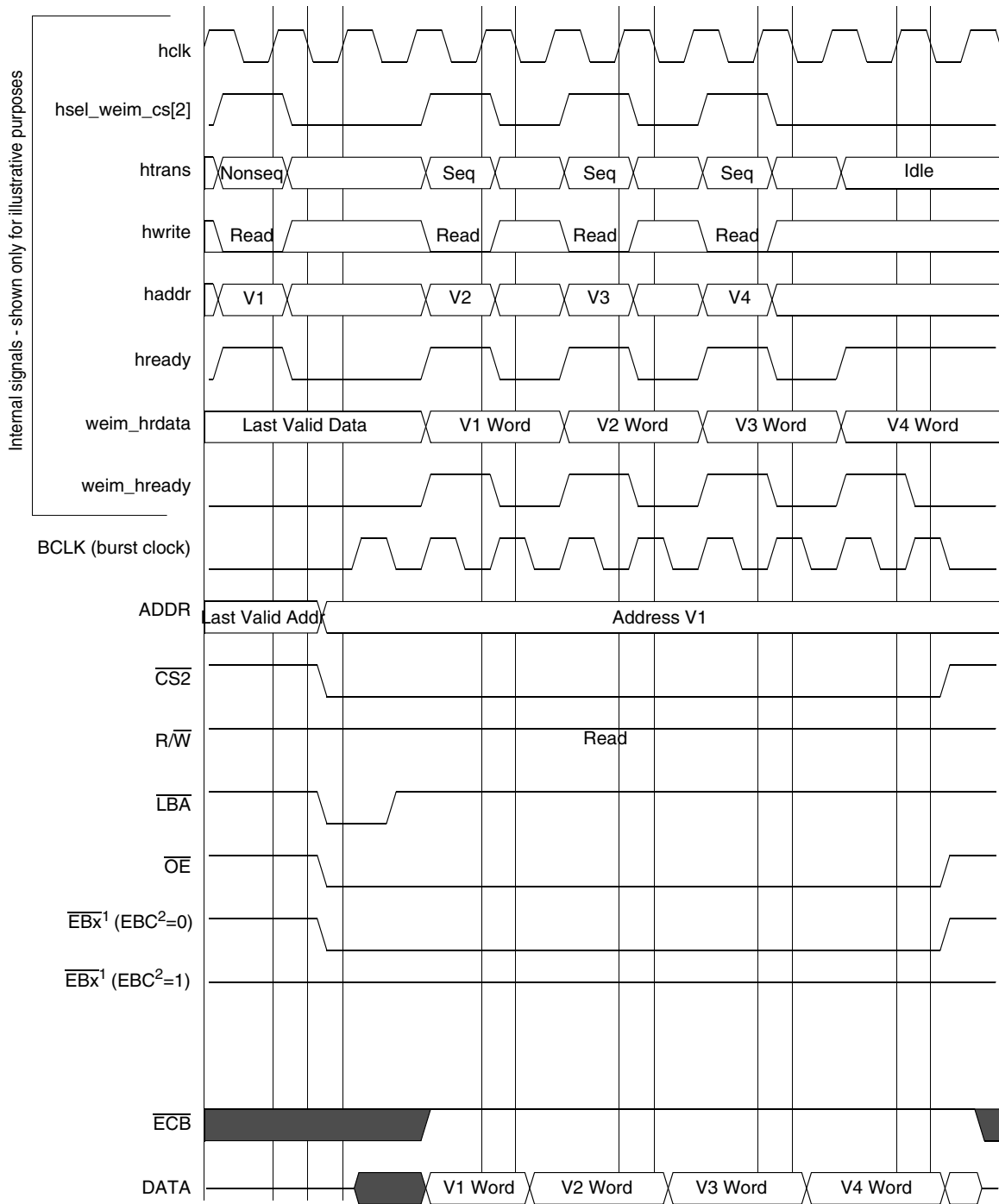
Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

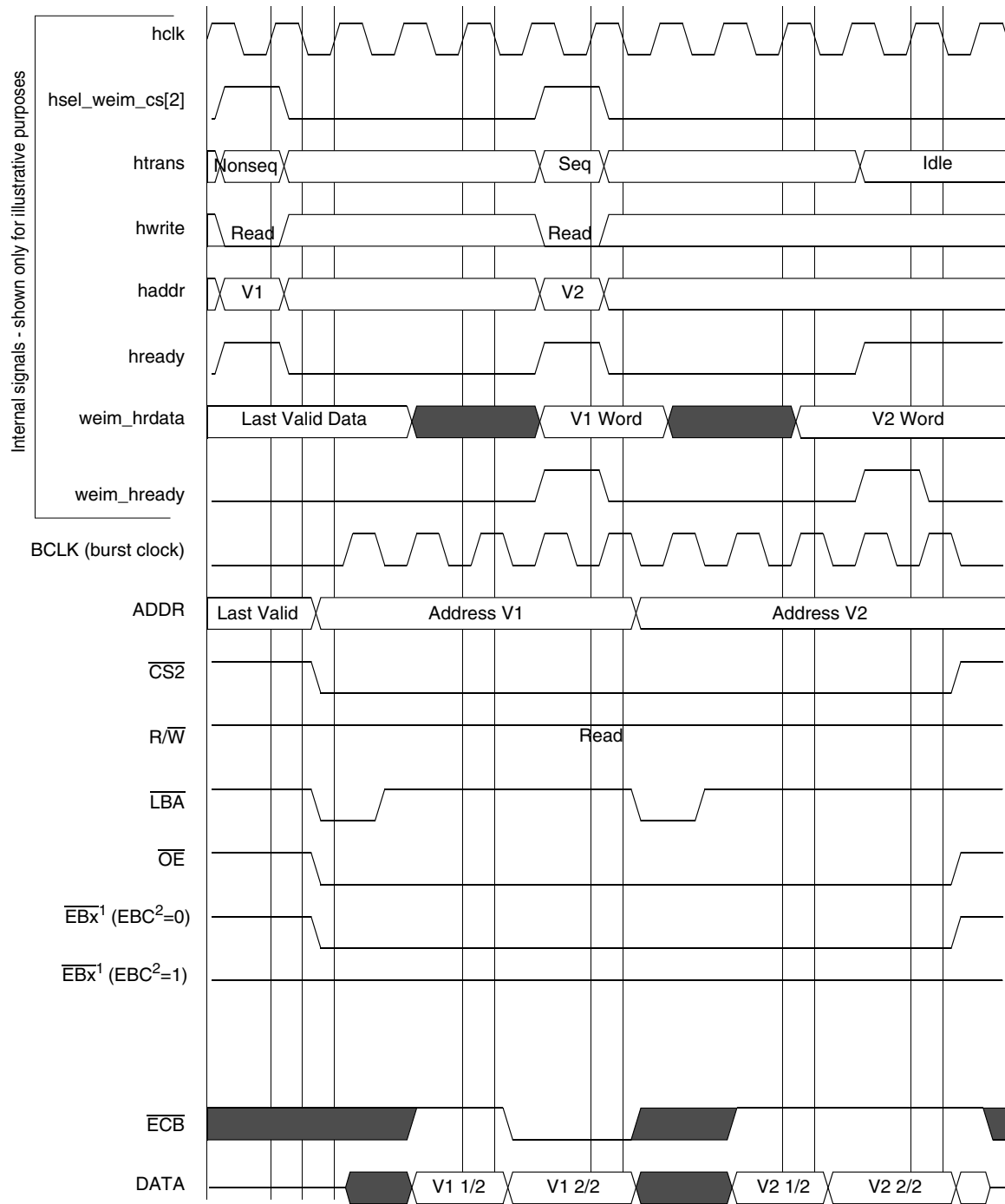
Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

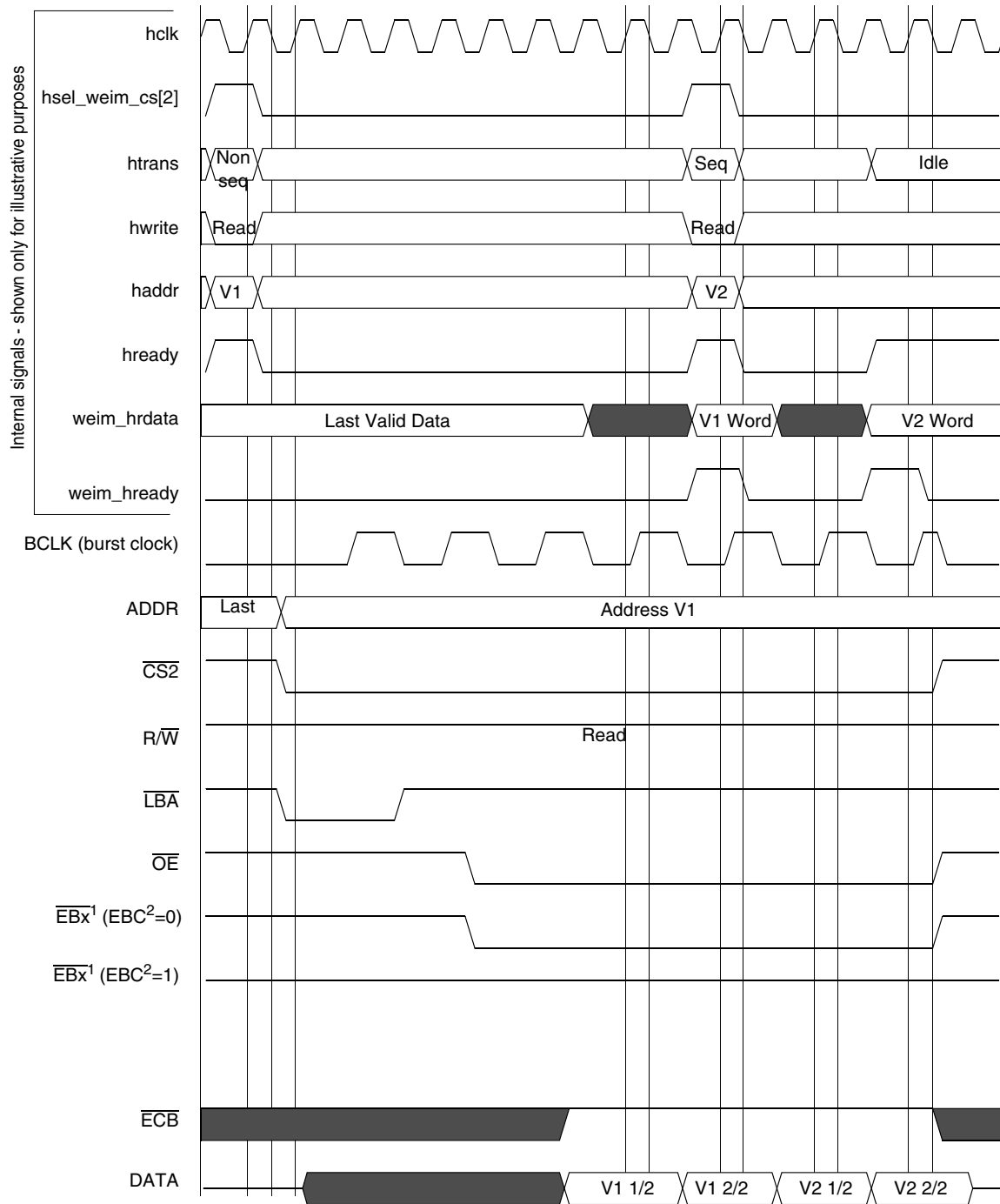
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

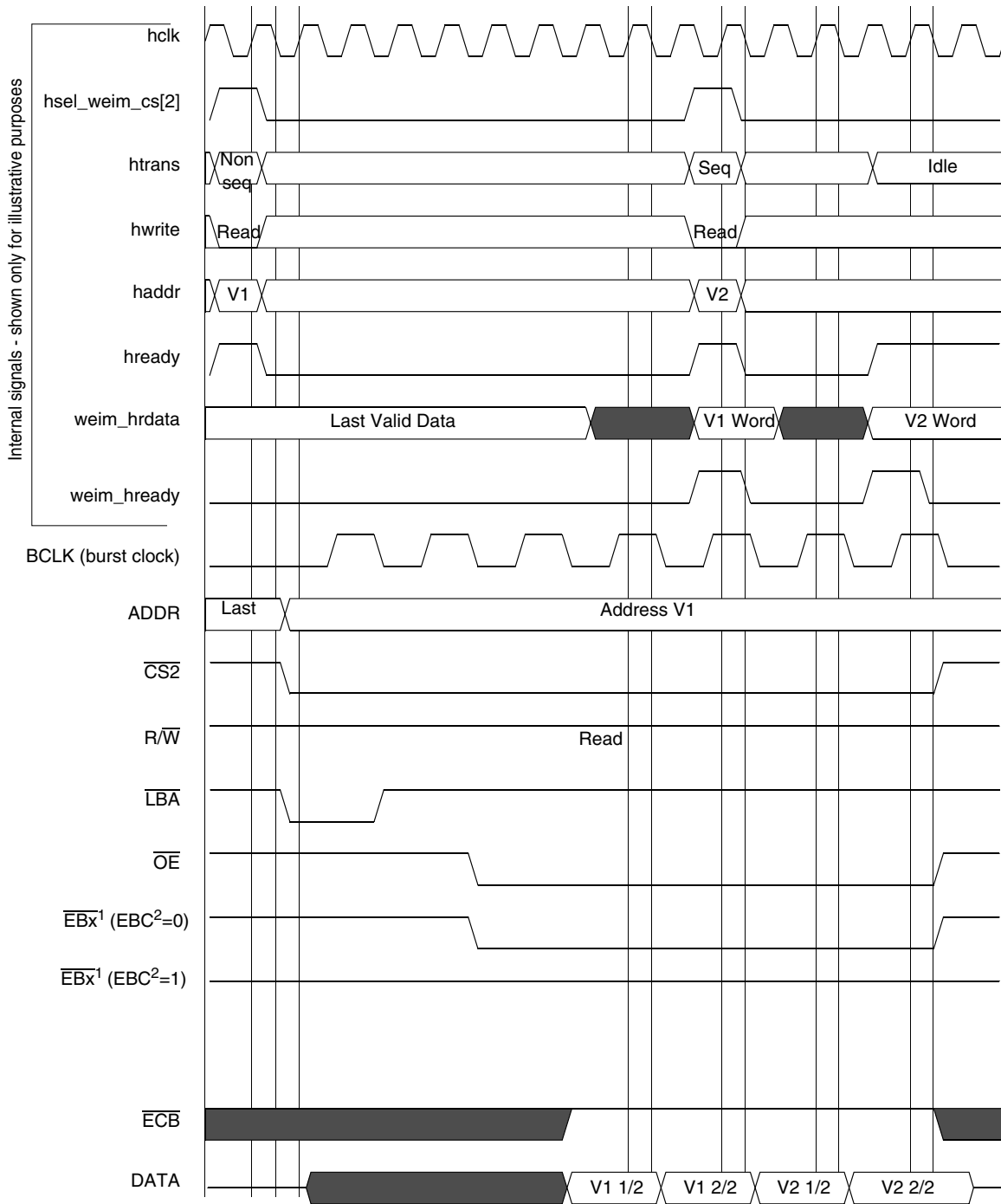
Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 31. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

4.4.4 Non-TFT Panel Timing

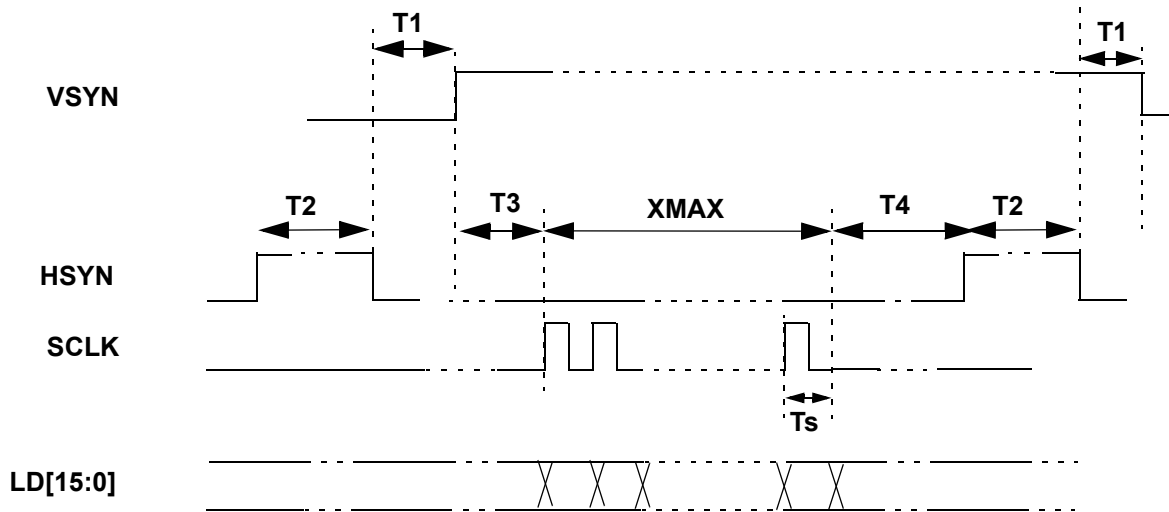


Figure 33. Non-TFT Panel Timing

Table 16. Non TFT Panel Timing Diagram

Symbol	Parameter	Allowed Register Minimum Value ^{1, 2}	Actual Value	Unit
T1	HSYN to VSYN delay ³	0	HWAIT2+2	Tpix ⁴
T2	HSYN pulse width	0	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts^5$	–
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

¹ Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.
² Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.
³ VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.
⁴ Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).
⁵ Ts is the shift clock period. Ts = Tpix * (panel data bus width).

4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the \overline{SS} signal (output) and the $\overline{SPI_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) and the SPI2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, \overline{SS} becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

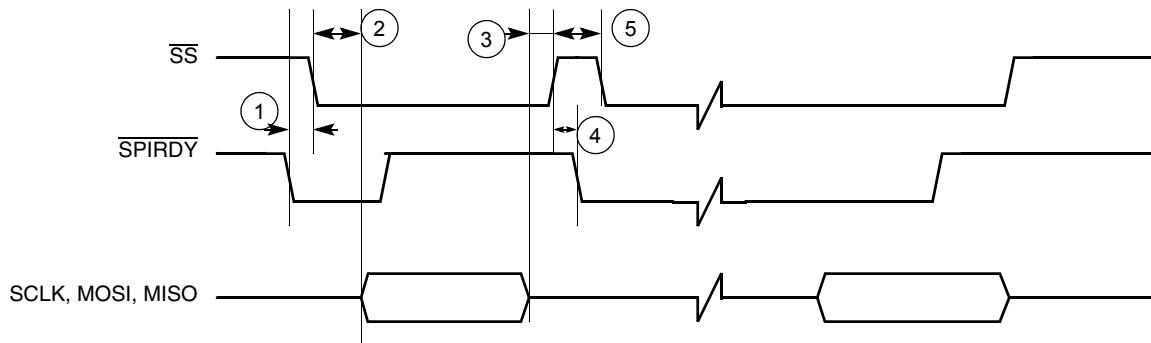


Figure 34. Master SPI Timing Diagram Using $\overline{SPI_RDY}$ Edge Trigger

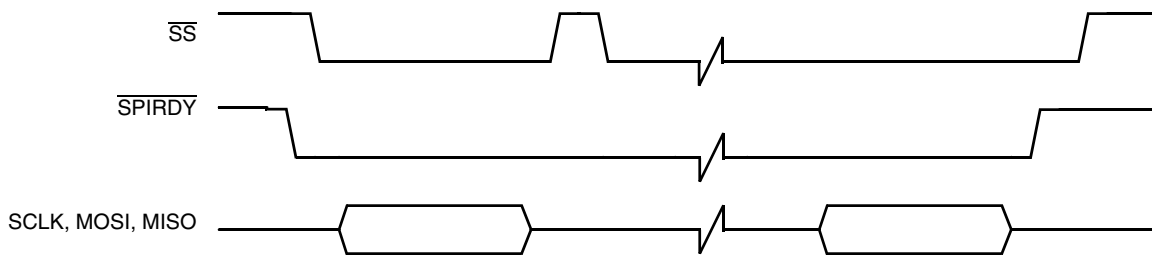


Figure 35. Master SPI Timing Diagram Using $\overline{SPI_RDY}$ Level Trigger

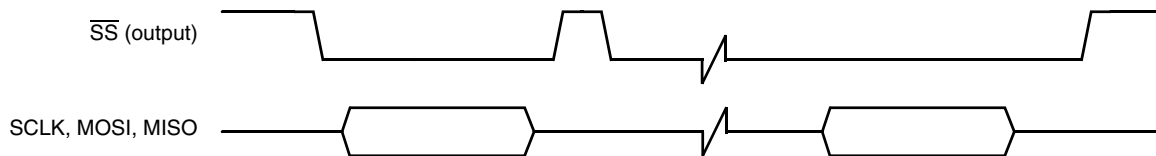


Figure 36. Master SPI Timing Diagram Ignore $\overline{SPI_RDY}$ Level Trigger

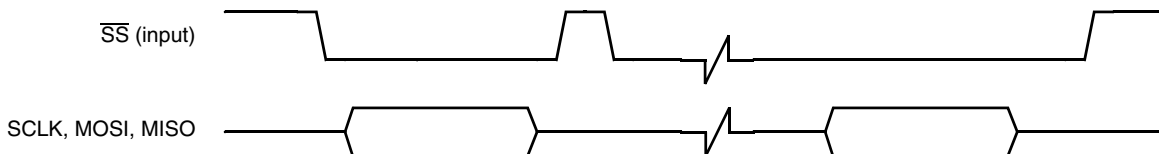


Figure 37. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

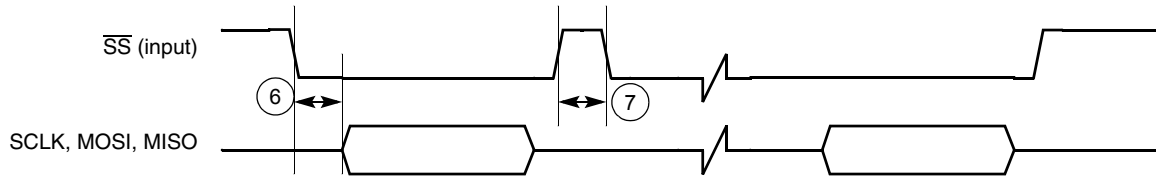


Figure 38. Slave SPI Timing Diagram FIFO Advanced by \overline{SS} Rising Edge

Table 17. Timing Parameter Table for Figure 34 through Figure 38

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{SPI_RDY}$ to \overline{SS} output low	$2T^1$	–	ns
2	\overline{SS} output low to first SCLK edge	$3 \cdot T_{sclk}^2$	–	ns
3	Last SCLK edge to \overline{SS} output high	$2 \cdot T_{sclk}$	–	ns
4	\overline{SS} output high to $\overline{SPI_RDY}$ low	0	–	ns
5	\overline{SS} output pulse width	$T_{sclk} + WAIT^3$	–	ns
6	\overline{SS} input low to first SCLK edge	T	–	ns
7	\overline{SS} input pulse width	T	–	ns

¹ T = CSPI system clock period (PERCLK2).

² T_{sclk} = Period of SCLK.

³ WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

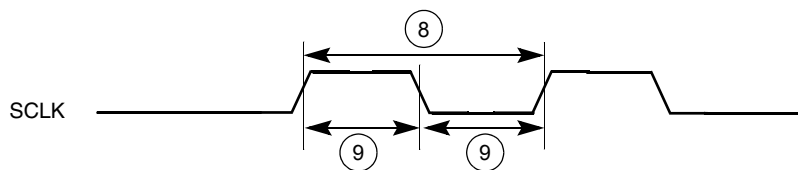


Figure 39. SPI SCLK Timing Diagram

Table 18. Timing Parameter Table for SPI SCLK

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
8	SCLK frequency	0	10	MHz
9	SCLK pulse width	100	–	ns

4.6 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MXL Reference Manual*.

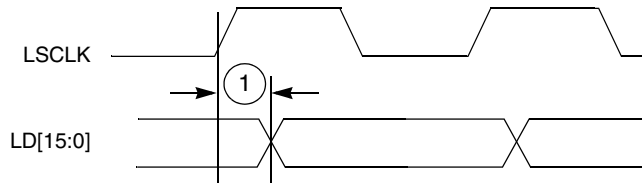


Figure 40. SCLK to LD Timing Diagram

Table 19. LCDC SCLK Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	SCLK to LD valid	-	2	ns

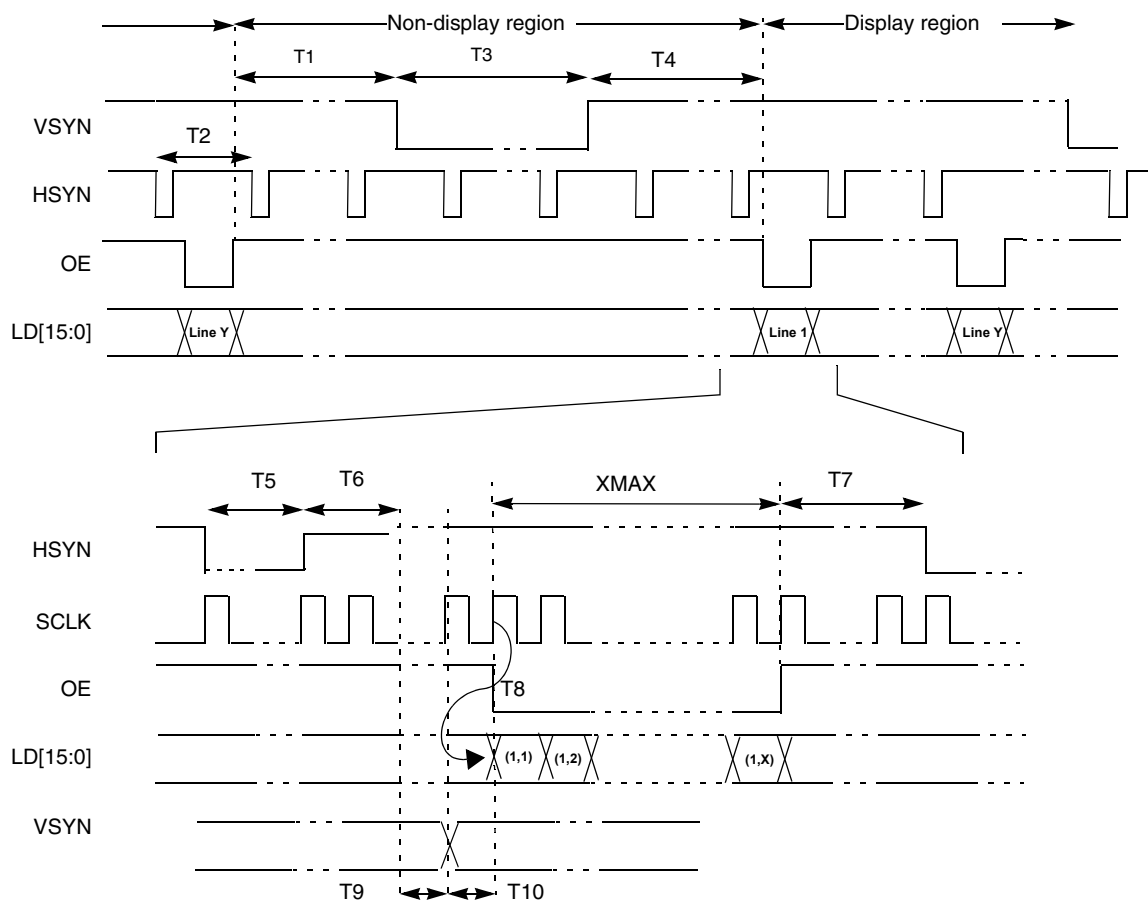


Figure 41. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Table 20. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Corresponding Register Value	Unit
T1	End of OE to beginning of VSYN	$T5+T6+T7+T9$	$(VWAIT1 \cdot T2)+T5+T6+T7+T9$	Ts
T2	HSYN period	$XMAX+5$	$XMAX+T5+T6+T7+T9+T10$	Ts
T3	VSYN pulse width	T2	$VWIDTH \cdot (T2)$	Ts
T4	End of VSYN to beginning of OE	2	$VWAIT2 \cdot (T2)$	Ts
T5	HSYN pulse width	1	$HWIDTH+1$	Ts
T6	End of HSYN to beginning to T9	1	$HWAIT2+1$	Ts
T7	End of OE to beginning of HSYN	1	$HWAIT1+1$	Ts
T8	SCLK to valid LD data	-3	3	ns
T9	End of HSYN idle2 to VSYN edge (for non-display region)	2	2	Ts
T9	End of HSYN idle2 to VSYN edge (for Display region)	1	1	Ts
T10	VSYN to OE active (Sharp = 0) when VWAIT2 = 0	1	1	Ts
T10	VSYN to OE active (Sharp = 1) when VWAIT2 = 0	2	2	Ts

Note:

- Ts is the SCLK period which equals $LCDC_CLK / (PCD + 1)$. Normally $LCDC_CLK = 15ns$.
- VSYN, HSYN and OE can be programmed as active high or active low. In [Figure 41](#), all 3 signals are active low.
- The polarity of SCLK and LD[15:0] can also be programmed.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In [Figure 41](#), SCLK is always active.
- For T9 non-display region, VSYN is non-active. It is used as a reference.
- XMAX is defined in pixels.

4.7 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

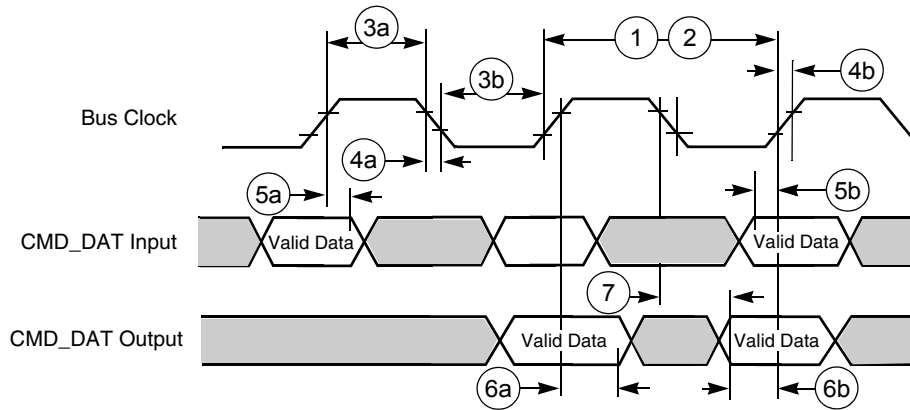


Figure 42. Chip-Select Read Cycle Timing Diagram

Table 21. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP) ¹ —10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode ²	0	400	0	400	kHz
3a	Clock high time ¹ —10/30 cards	6/33	—	10/50	—	ns
3b	Clock low time ¹ —10/30 cards	15/75	—	10/50	—	ns
4a	Clock fall time ¹ —10/30 cards	—	10/50 (5.00) ³	—	10/50	ns
4b	Clock rise time ¹ —10/30 cards	—	14/67 (6.67) ³	—	10/50	ns
5a	Input hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
5b	Input setup time ³ —10/30 cards	10.3	—	9/9	—	ns
6a	Output hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
6b	Output setup time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
7	Output delay time ³	0	16	0	14	ns

¹ C_L ≤ 100 pF / 250 pF (10/30 cards)

² C_L ≤ 250 pF (21 cards)

³ C_L ≤ 25 pF (1 card)

4.7.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is N_{CR} clock cycles as illustrated in Figure 43. The symbols for Figure 43 through Figure 47 are defined in Table 22.

Table 22. State Signal Parameters for Figure 43 through Figure 47

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

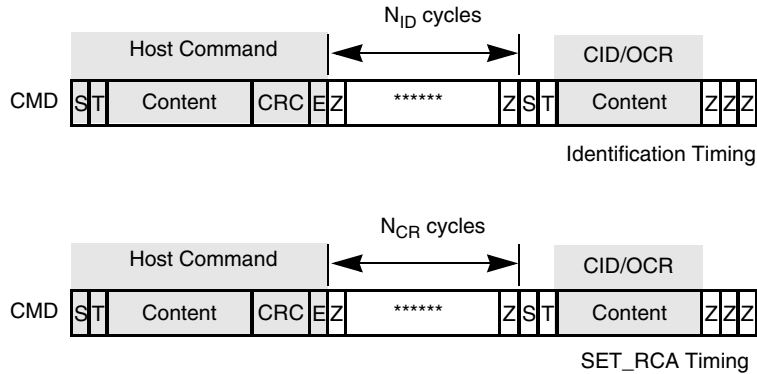


Figure 43. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 44, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC} .

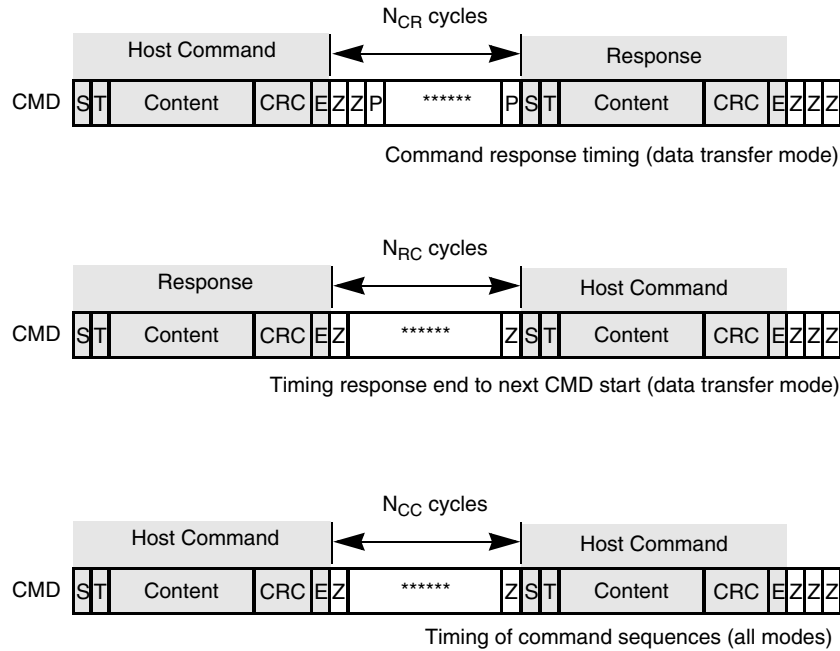


Figure 44. Timing Diagrams at Data Transfer Mode

Figure 45 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC} , beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

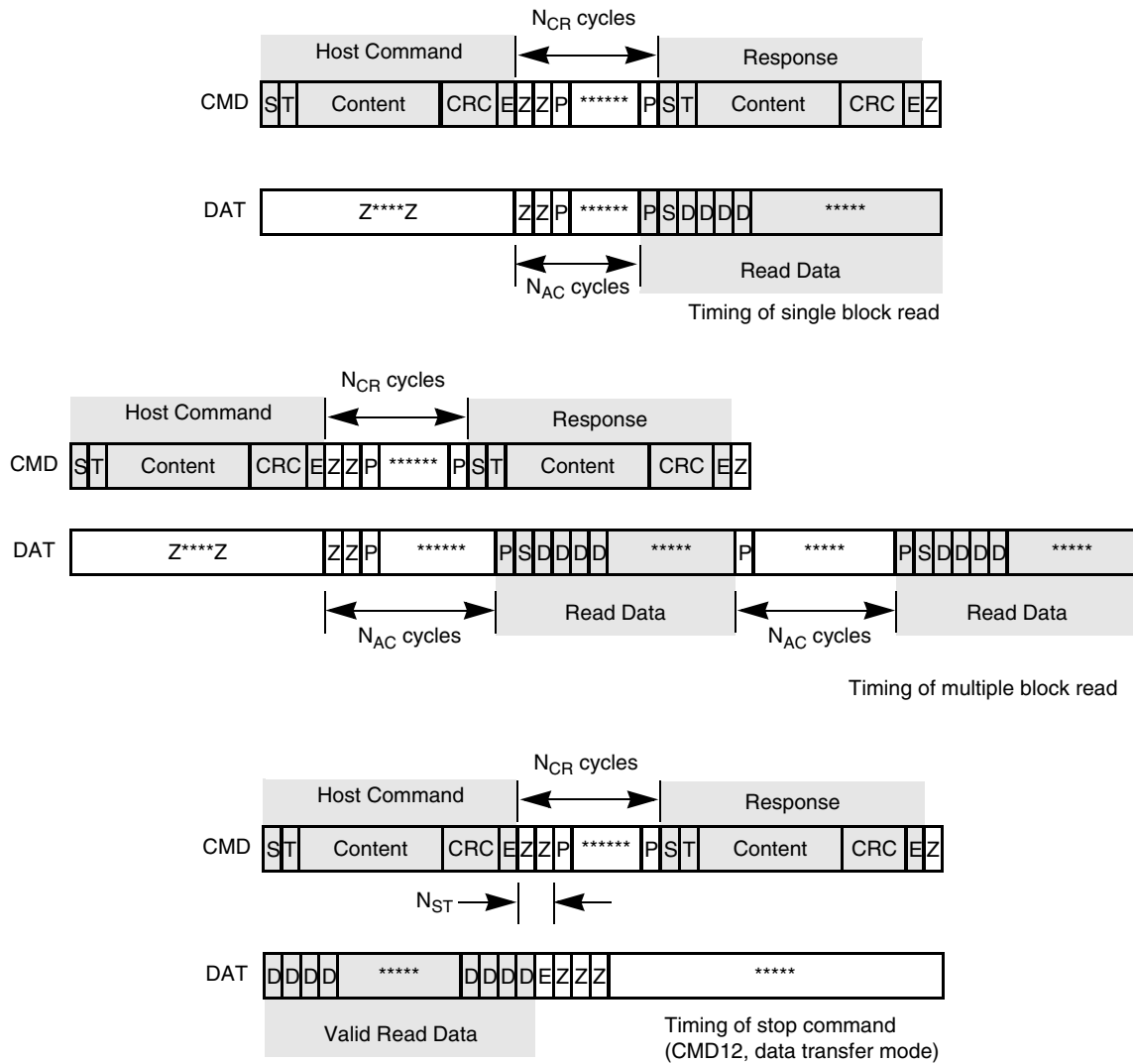


Figure 45. Timing Diagrams at Data Read

Figure 46 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

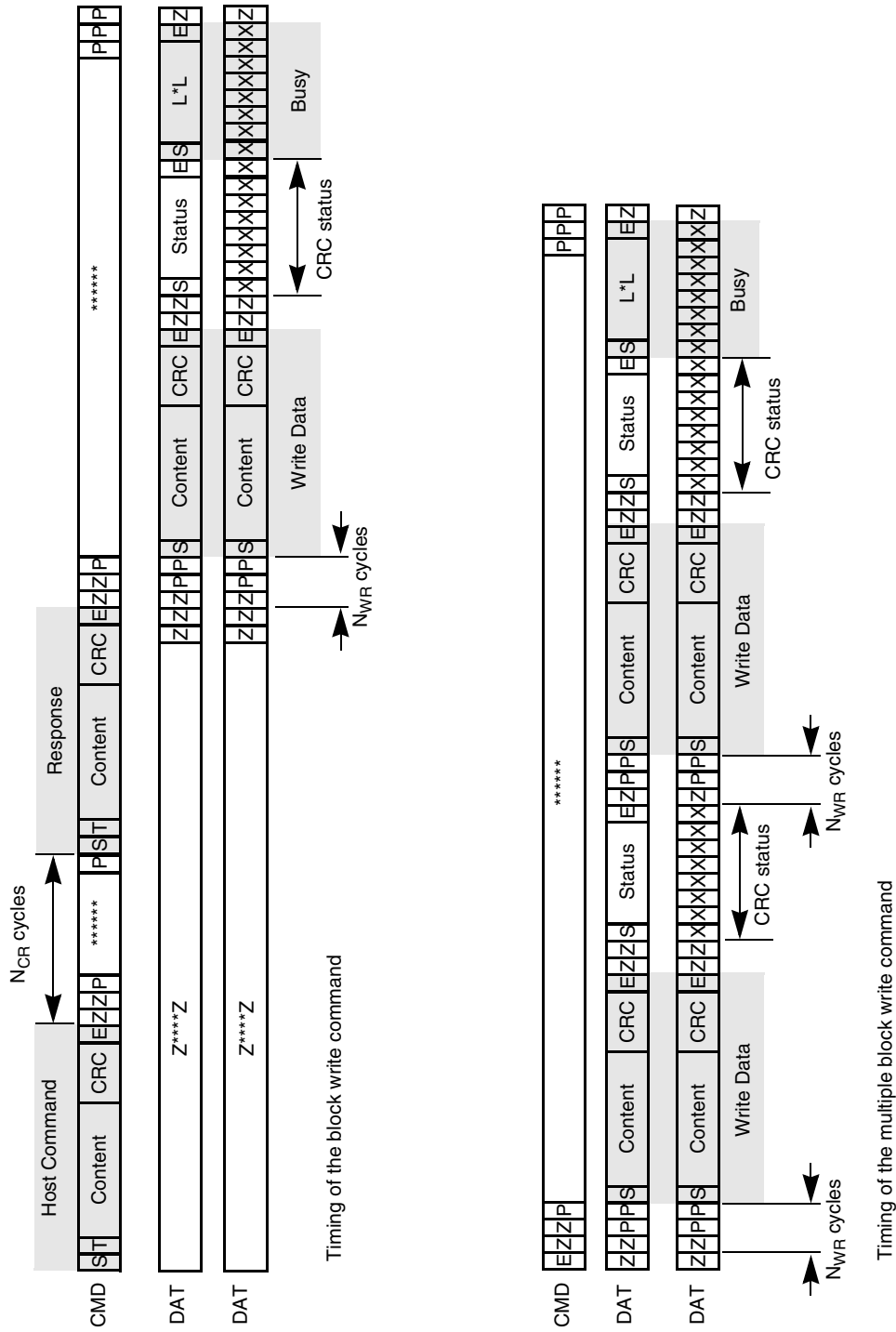


Figure 46. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 47 shows the different scenarios on the bus.

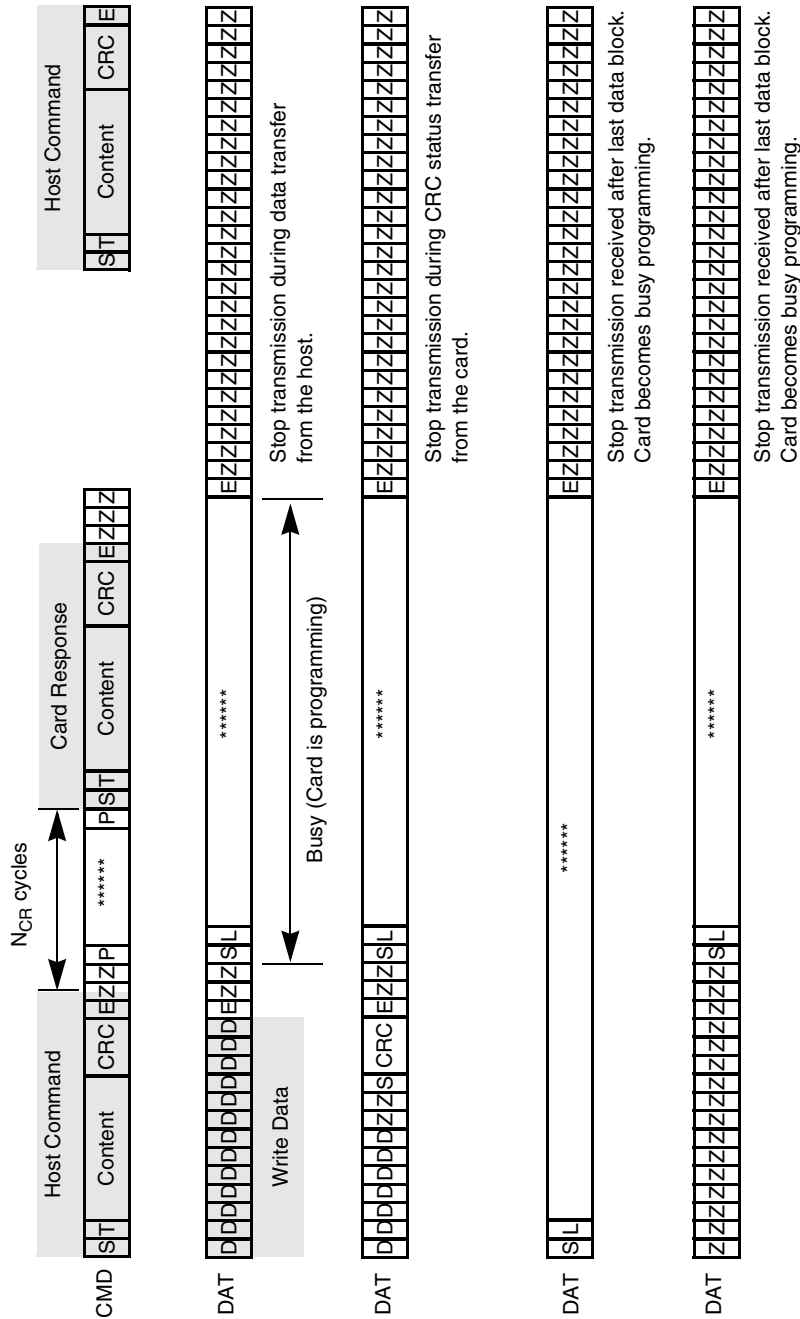


Figure 47. Stop Transmission During Different Scenarios

Table 23. Timing Values for Figure 43 through Figure 47

Parameter	Symbol	Minimum	Maximum	Unit
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL))				
Command response cycle	NCR	2	64	Clock cycles
Identification response cycle	NID	5	5	Clock cycles
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles

Table 23. Timing Values for Figure 43 through Figure 47 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112]				
NSAC: Data read access time -2 in CLK cycles (NSAC-100) defined in CSD register bit[111:104]				

4.7.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the "Interrupt Period" during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

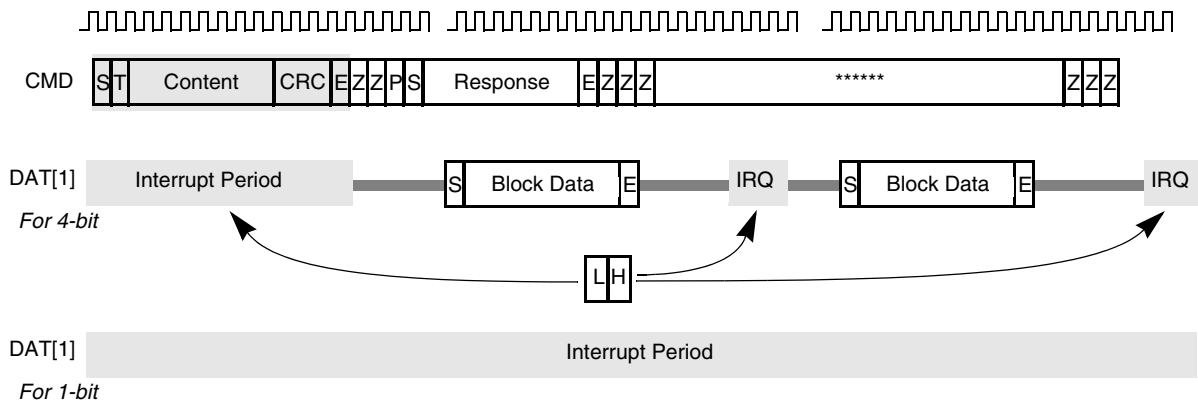


Figure 48. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

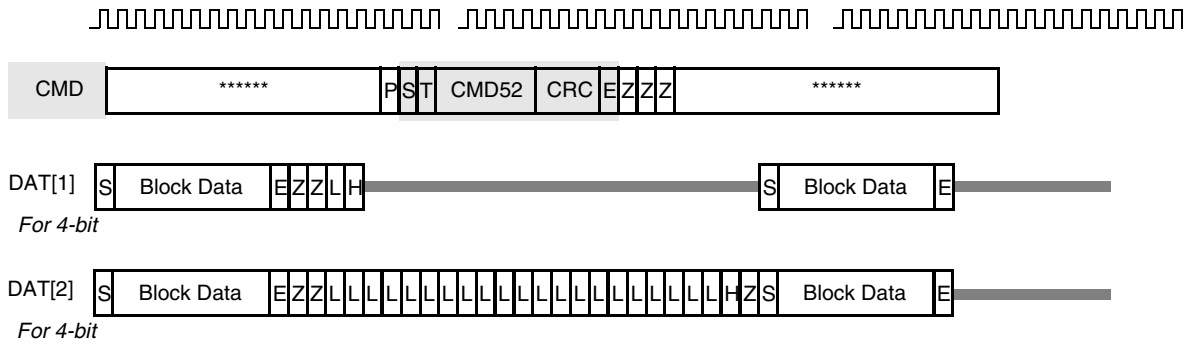


Figure 49. SDIO ReadWait Timing Diagram

4.8 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

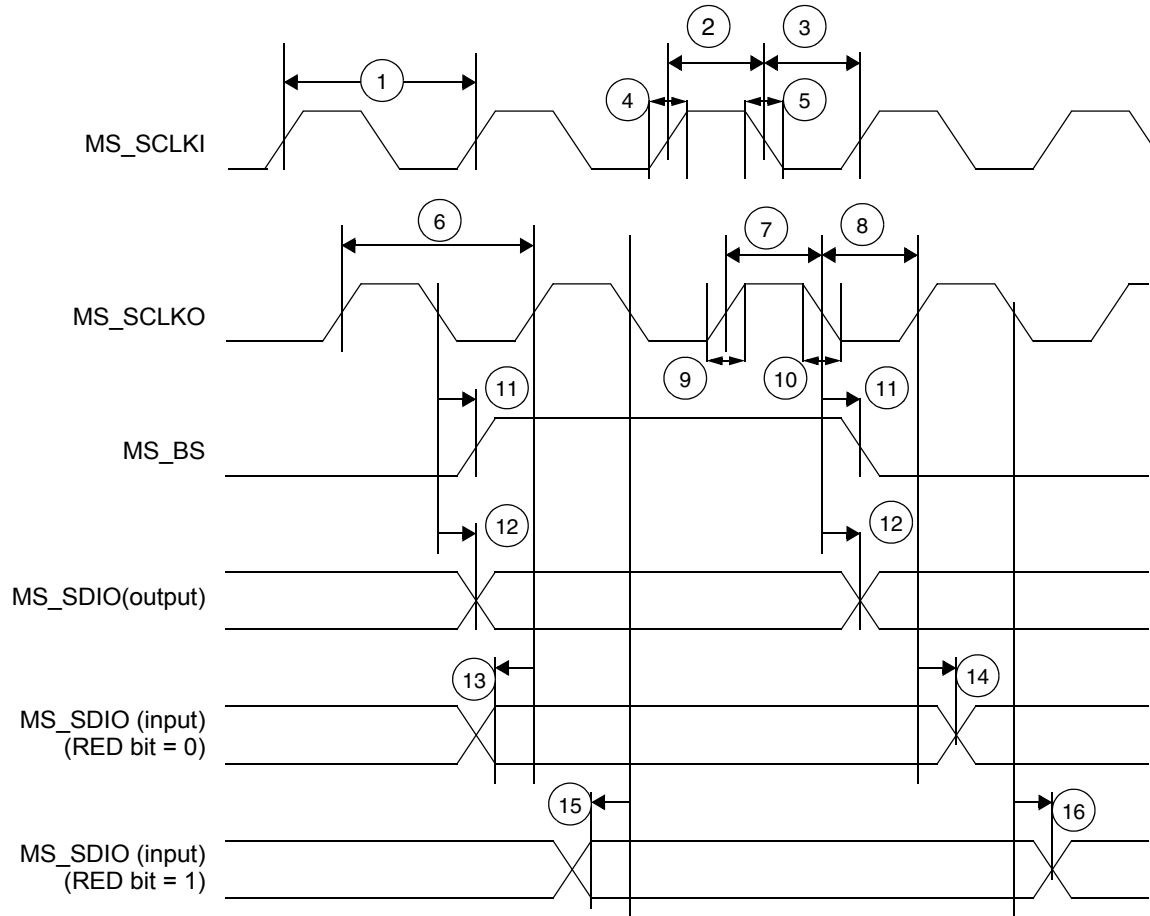


Figure 50. MSHC Signal Timing Diagram

Table 24. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency ¹	–	25	MHz
7	MS_SCLKO high pulse width ¹	20	–	ns
8	MS_SCLKO low pulse width ¹	15	–	ns
9	MS_SCLKO rise time ¹	–	5	ns
10	MS_SCLKO fall time ¹	–	5	ns
11	MS_BS delay time ¹	–	3	ns

Table 24. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	MS_SDIO output delay time ^{1,2}	–	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0) ³	18	–	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0) ³	0	–	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1) ⁴	23	–	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1) ⁴	0	–	ns

¹ Loading capacitor condition is less than or equal to 30pF.

² An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.

³ If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.

⁴ If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

4.9 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in [Figure 51](#) and the parameters are listed in [Table 25](#).

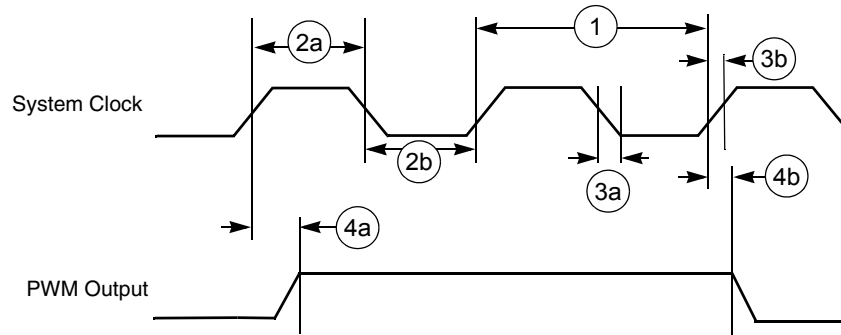


Figure 51. PWM Output Timing Diagram

Table 25. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency ¹	0	87	0	100	MHz
2a	Clock high time ¹	3.3	–	5/10	–	ns
2b	Clock low time ¹	7.5	–	5/10	–	ns
3a	Clock fall time ¹	–	5	–	5/10	ns
3b	Clock rise time ¹	–	6.67	–	5/10	ns
4a	Output delay time ¹	5.7	–	5	–	ns
4b	Output setup time ¹	5.7	–	5	–	ns

¹ C_L of PWMO = 30 pF

4.10 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.

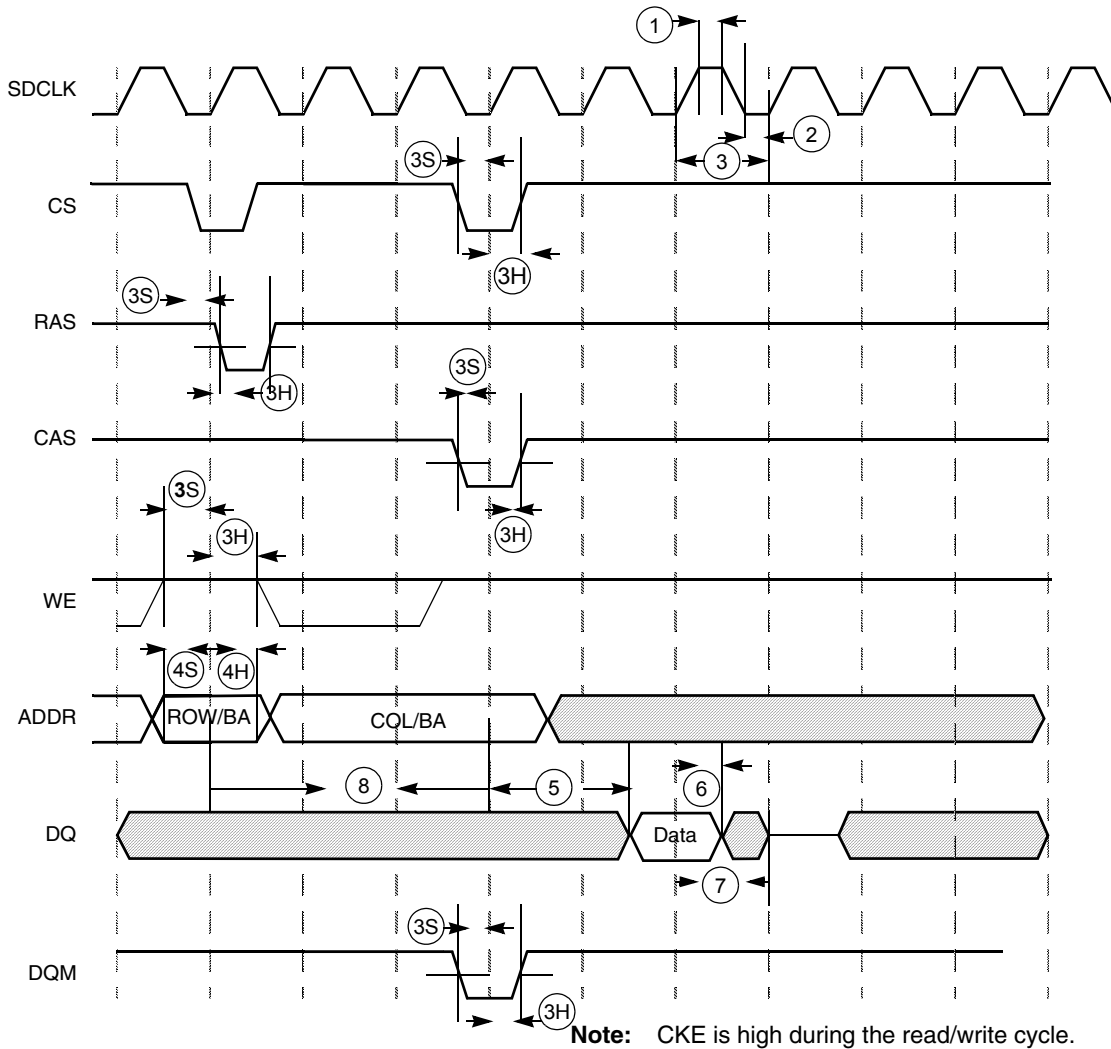


Figure 52. SDRAM Read Cycle Timing Diagram

Table 26. SDRAM Read Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	–	2	–	ns

Table 26. SDRAM Read Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
4S	Address setup time	3.42	–	3	–	ns
4H	Address hold time	2.28	–	2	–	ns
5	SDRAM access time (CL = 3)	–	6.84	–	6	ns
5	SDRAM access time (CL = 2)	–	6.84	–	6	ns
5	SDRAM access time (CL = 1)	–	22	–	22	ns
6	Data out hold time	2.85	–	2.5	–	ns
7	Data out high-impedance time (CL = 3)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 2)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 1)	–	22	–	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}^1	–	t_{RCD}^1	–	ns

¹ t_{RCD} = SDRAM clock cycle time. This settings can be found in the *MC9328MXL reference manual*.

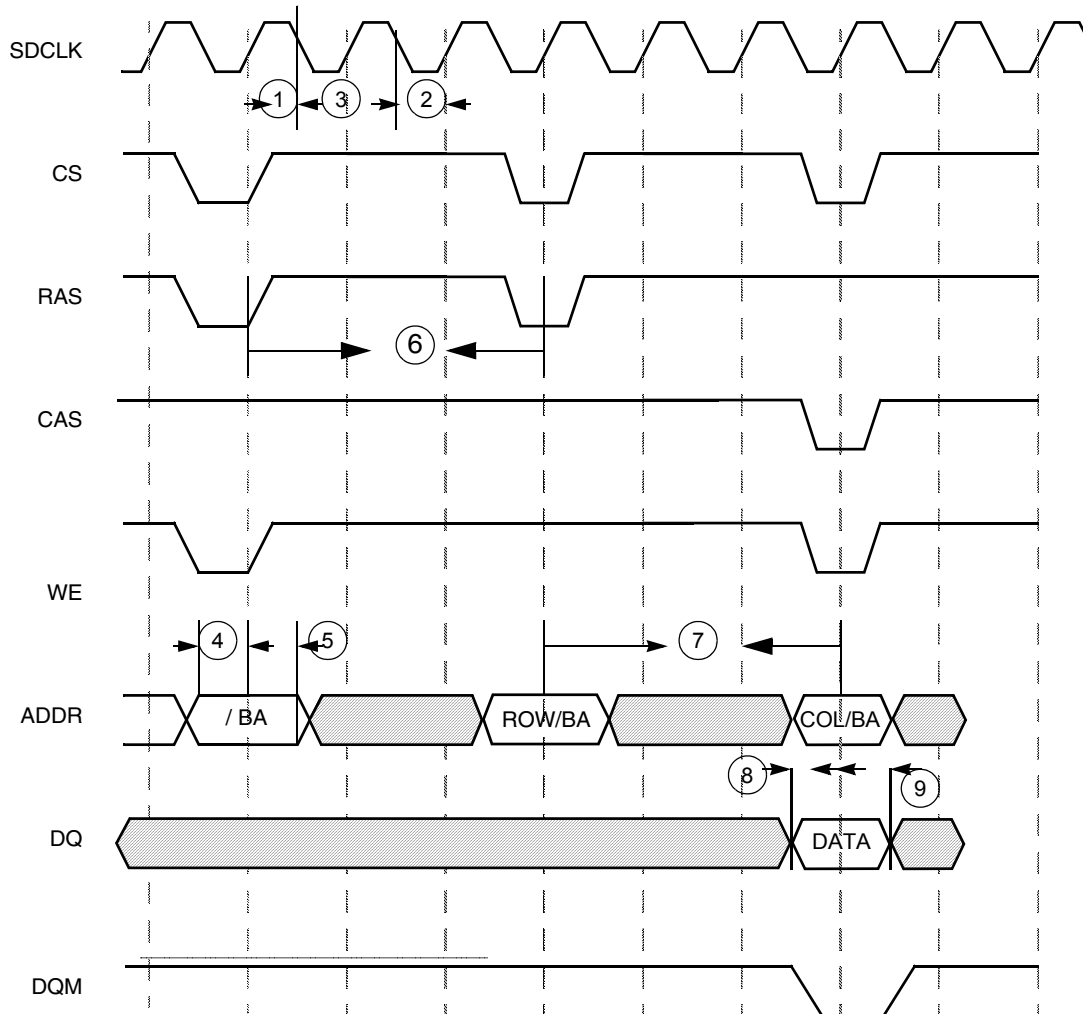


Figure 53. SDRAM Write Cycle Timing Diagram

Table 27. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period ¹	t_{RP}^2	–	t_{RP}^2	–	ns
7	Active to read/write command delay	t_{RCD}^2	–	t_{RCD}^2	–	ns

Table 27. SDRAM Write Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
8	Data setup time	4.0	–	2	–	ns
9	Data hold time	2.28	–	2	–	ns

¹ Precharge cycle timing is included in the write timing diagram.

² t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the *MC9328MXL reference manual*.

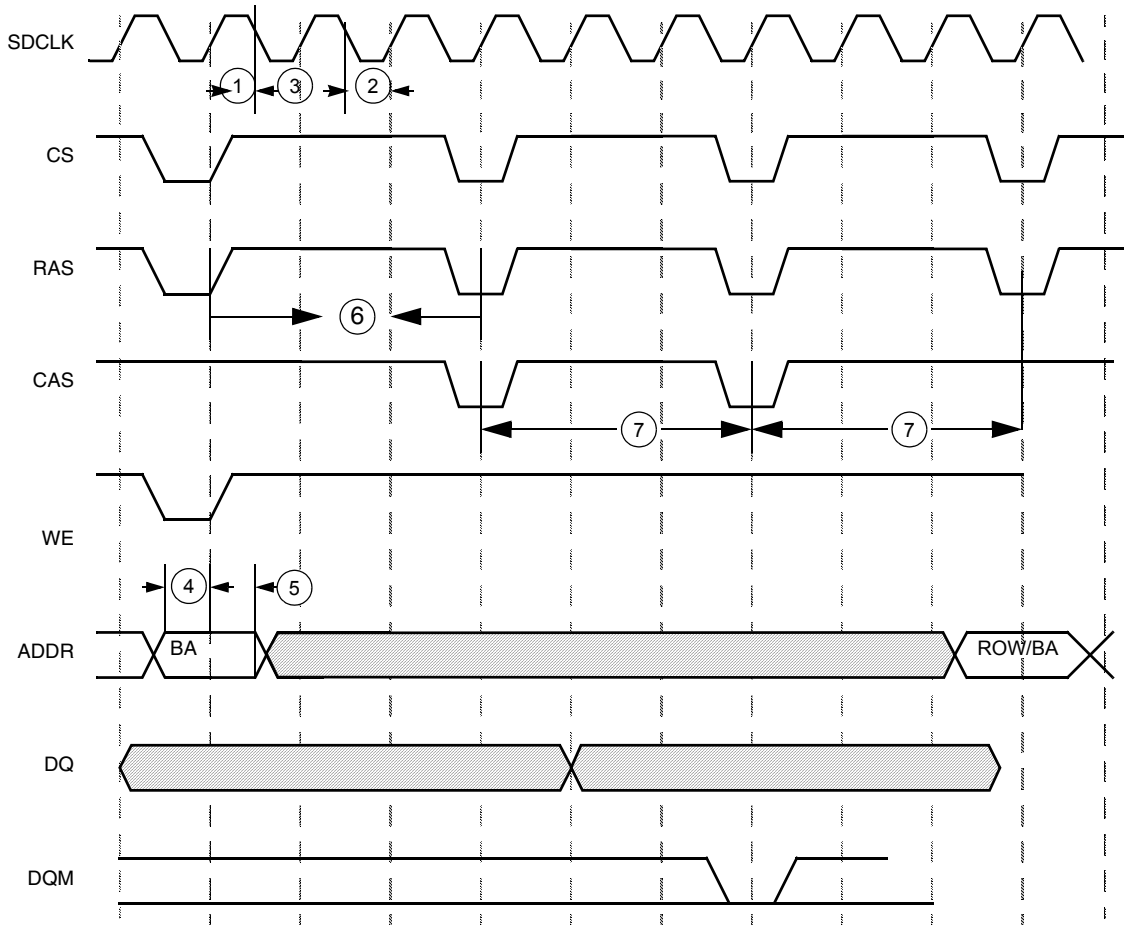


Figure 54. SDRAM Refresh Timing Diagram

Table 28. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns

Table 28. SDRAM Refresh Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}^1	–	t_{RP}^1	–	ns
7	Auto precharge command period	t_{RC}^1	–	t_{RC}^1	–	ns

¹ t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MXL reference manual*.

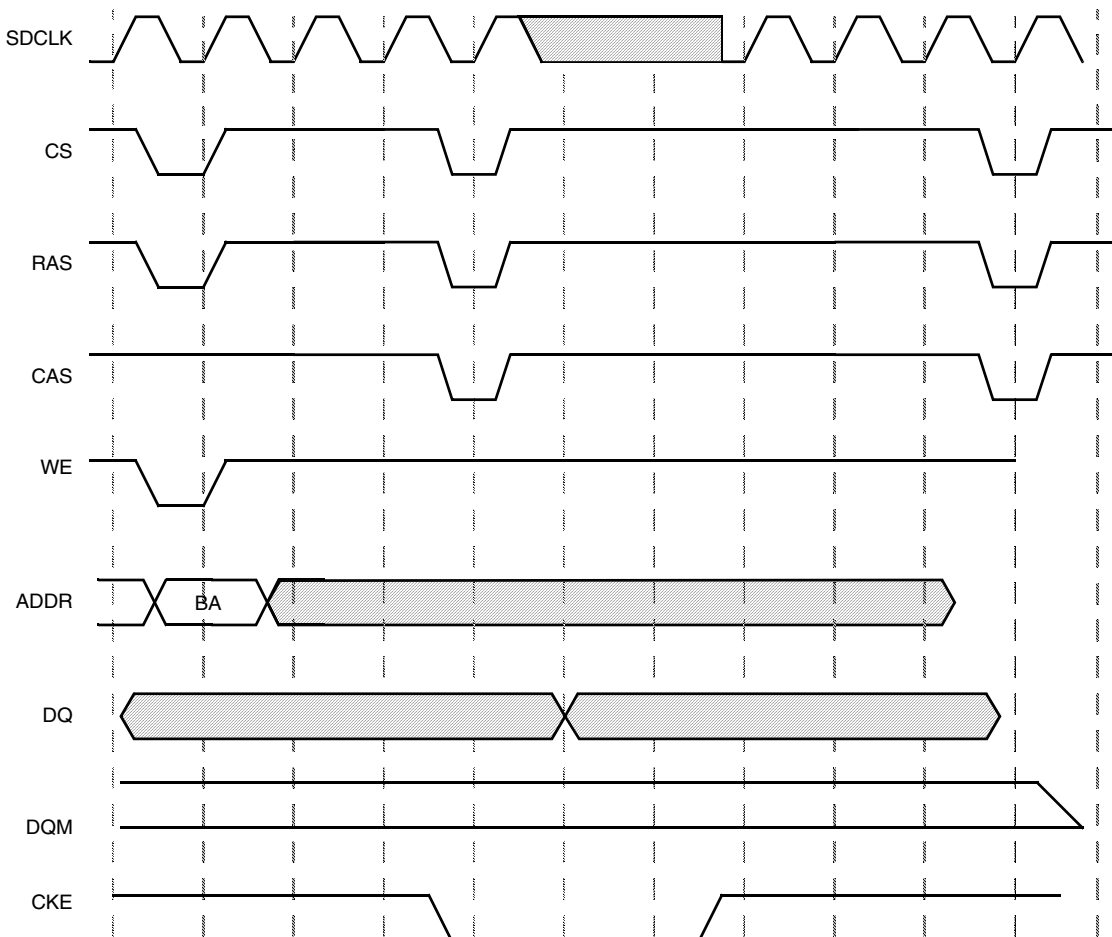


Figure 55. SDRAM Self-Refresh Cycle Timing Diagram

4.11 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

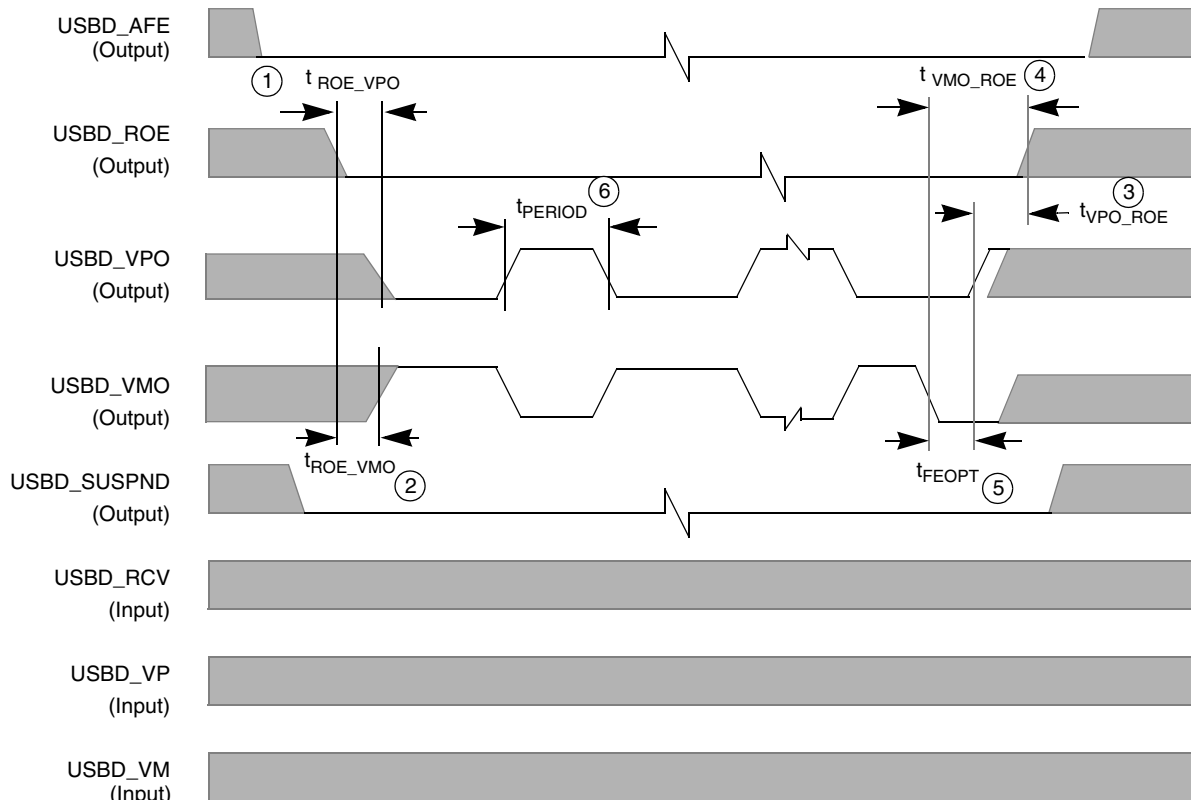


Figure 56. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 29. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{ROE_VPO} : USBD_ROE active to USBD_VPO low	83.14	83.47	ns
2	t_{ROE_VMO} : USBD_ROE active to USBD_VMO high	81.55	81.98	ns
3	t_{VPO_ROE} : USBD_VPO high to USBD_ROE deactivated	83.54	83.80	ns
4	t_{VMO_ROE} : USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.90	249.13	ns

Table 29. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX) (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
5	t _{FEOPT} ; SE0 interval of EOP	160.00	175.00	ns
6	t _{PERIOD} ; Data transfer rate	11.97	12.03	Mb/s

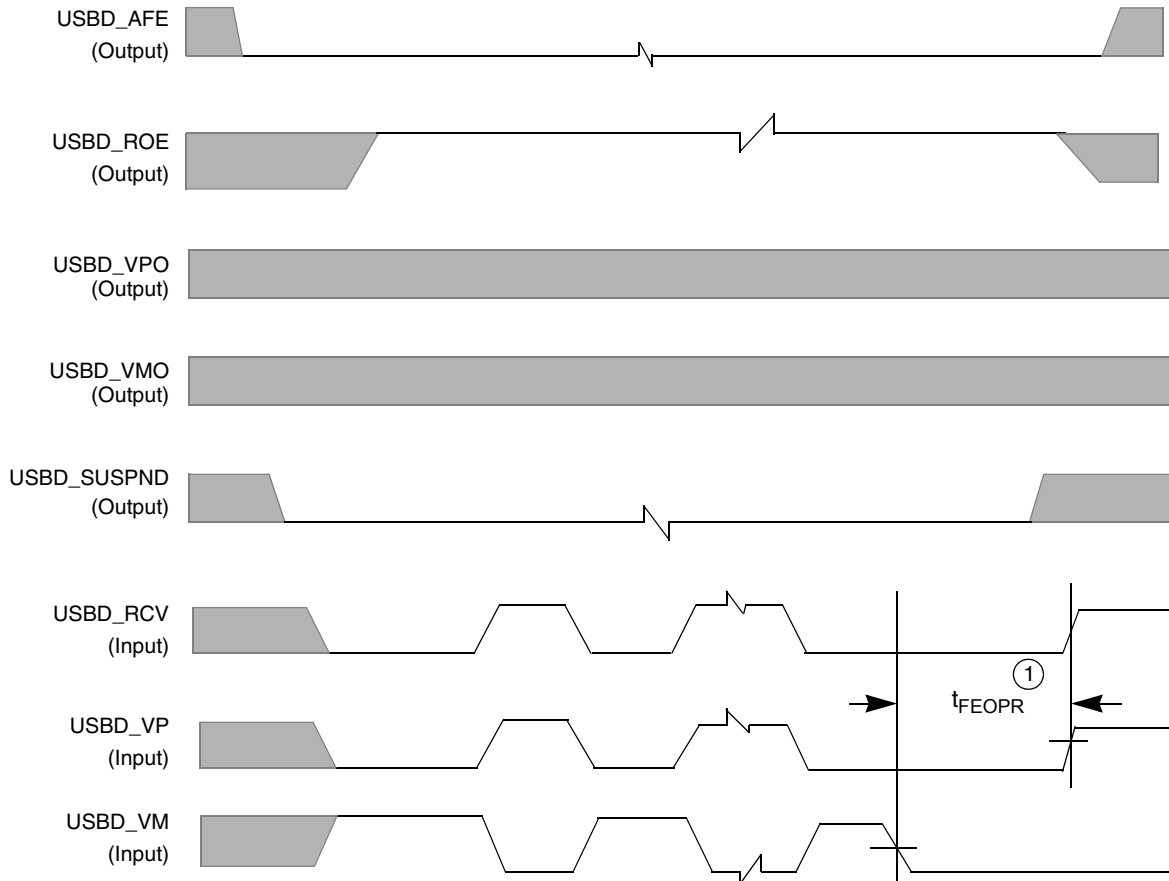


Figure 57. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 30. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t _{FEOPR} ; Receiver SE0 interval of EOP	82	–	ns

4.12 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

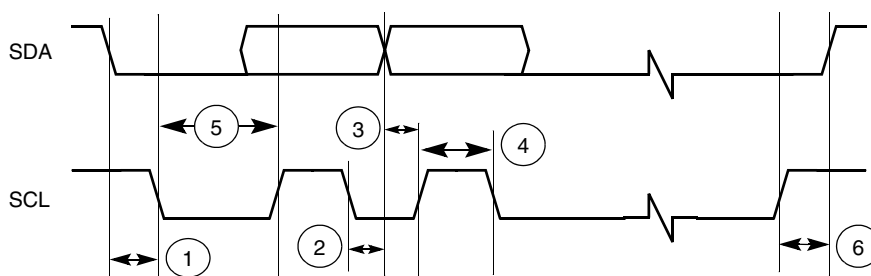


Figure 58. Definition of Bus Timing for I²C

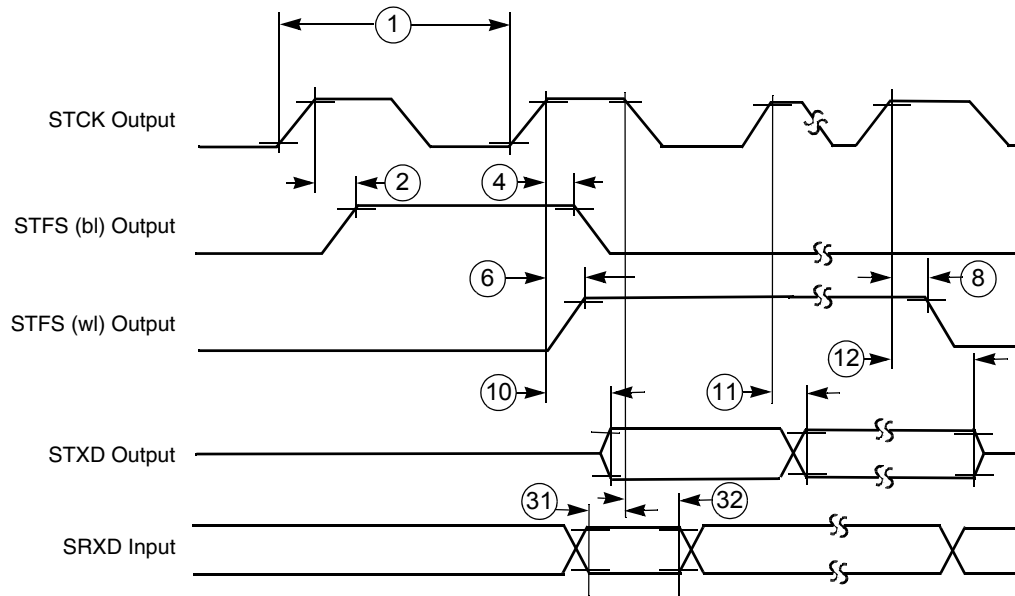
Table 31. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	–	160	–	ns
2	Data hold time	0	171	0	150	ns
3	Data setup time	11.4	–	10	–	ns
4	HIGH period of the SCL clock	80	–	120	–	ns
5	LOW period of the SCL clock	480	–	320	–	ns
6	Setup time for STOP condition	182.4	–	160	–	ns

4.13 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in [Figure 60](#) through [Figure 62](#).

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 59. SSI Transmitter Internal Clock Timing Diagram

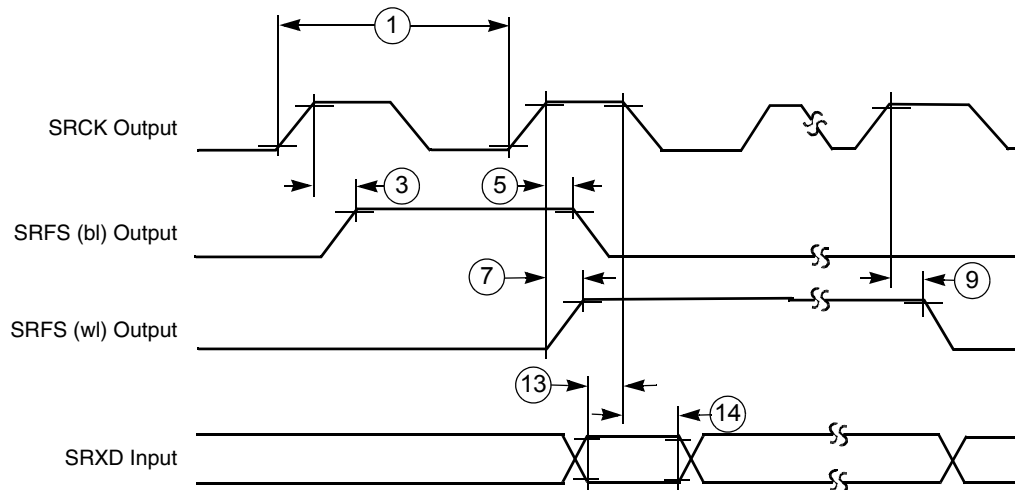
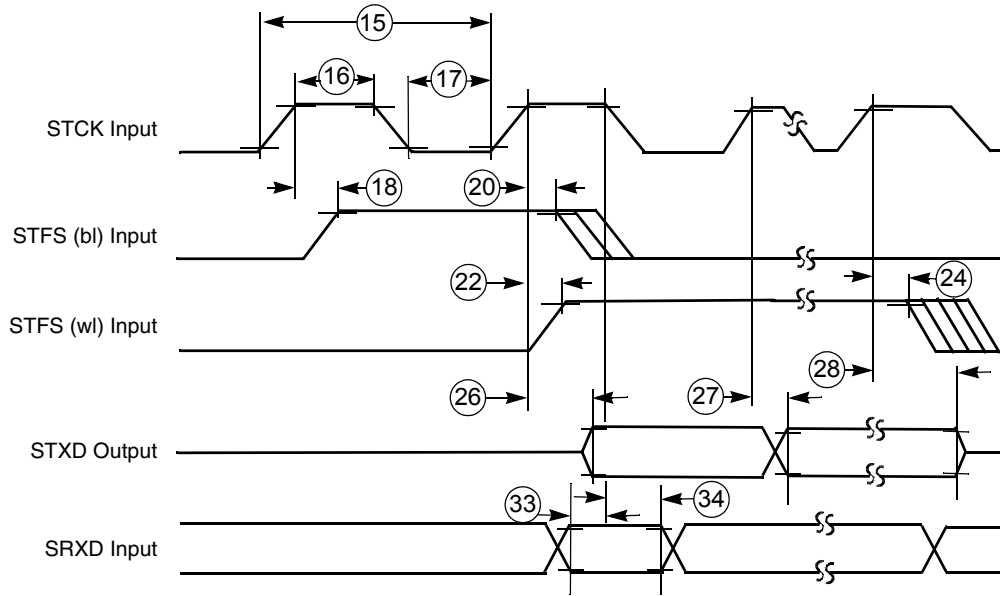


Figure 60. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 61. SSI Transmitter External Clock Timing Diagram

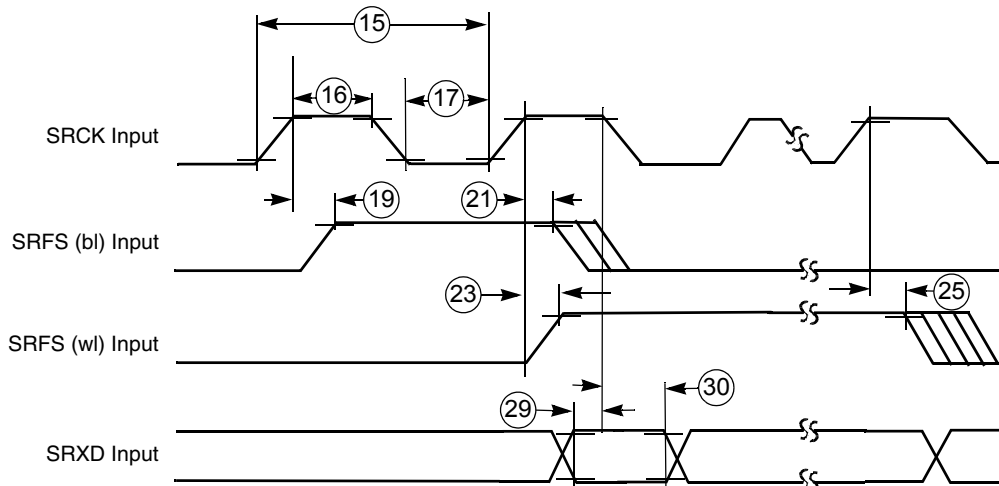


Figure 62. SSI Receiver External Clock Timing Diagram

Table 32. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation¹ (Port C Primary Function²)						
1	STCK/SRCK clock period ¹	95	–	83.3	–	ns
2	STCK high to STFS (bl) high ³	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high ³	-1.2	-1.7	-1.1	-1.5	ns
4	STCK high to STFS (bl) low ³	2.5	4.3	2.2	3.8	ns

Table 32. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
5	SRCK high to SRFS (bl) low ³	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high ³	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high ³	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low ³	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low ³	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function²)						
15	STCK/SRCK clock period ¹	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high ³	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function²)						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns

Table 32. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function²)						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

¹ All the timings for the SSI are given for a non-inverted serial clock polarity (TCKP/RCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

² There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

³ bl = bit length; wl = word length.

Table 33. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation¹ (Port B Alternate Function²)						
1	STCK/SRCK clock period ¹	95	–	83.3	–	ns
2	STCK high to STFS (bl) high ³	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high ³	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low ³	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low ³	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high ³	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high ³	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low ³	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low ³	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns

Table 33. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
External Clock Operation (Port B Alternate Function²)						
15	STCK/SRCK clock period ¹	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high ³	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hold time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port B Alternate Function²)						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port B Alternate Function²)						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

¹ All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

² There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

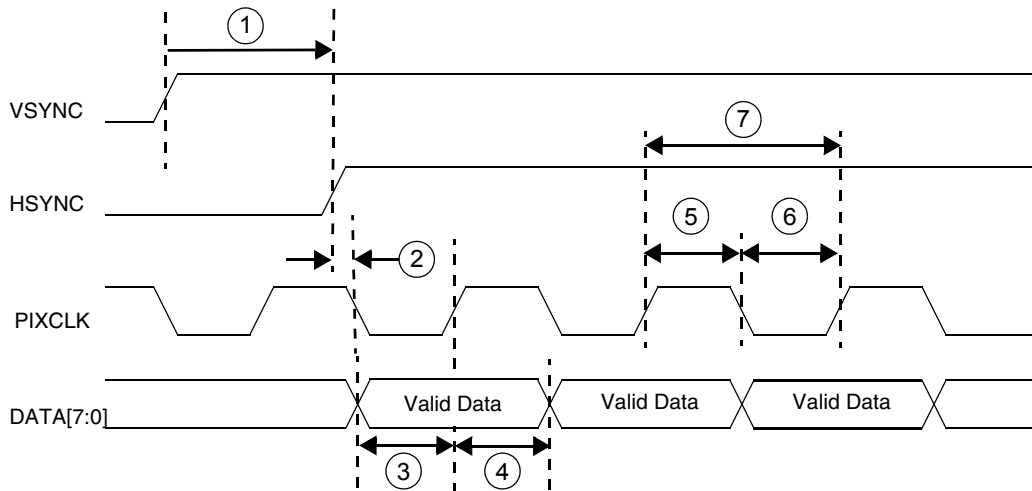
³ bl = bit length; wl = word length.

4.14 CMOS Sensor Interface

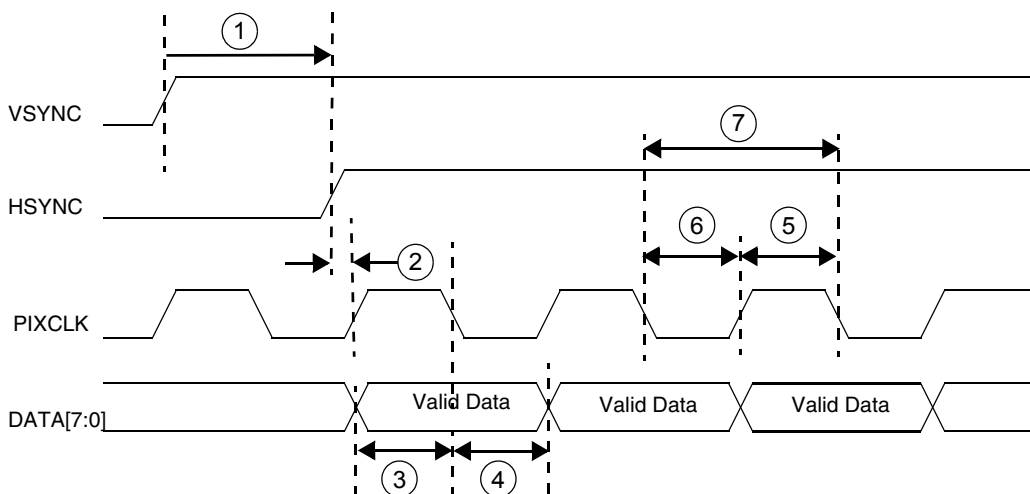
The CMOS Sensor Interface (CSI) module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32×32 image data receive FIFO, and a 16×32 statistic data FIFO.

4.14.1 Gated Clock Mode

Figure 63 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 64 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 34.



**Figure 63. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 64. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 34. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

$$\begin{aligned} \text{max rise time allowed} &= (\text{positive duty cycle} - \text{hold time}) \\ \text{max fall time allowed} &= (\text{negative duty cycle} - \text{setup time}) \end{aligned}$$

In most of case, duty cycle is 50 / 50, therefore

$$\begin{aligned} \text{max rise time} &= (\text{period} / 2 - \text{hold time}) \\ \text{max fall time} &= (\text{period} / 2 - \text{setup time}) \end{aligned}$$

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

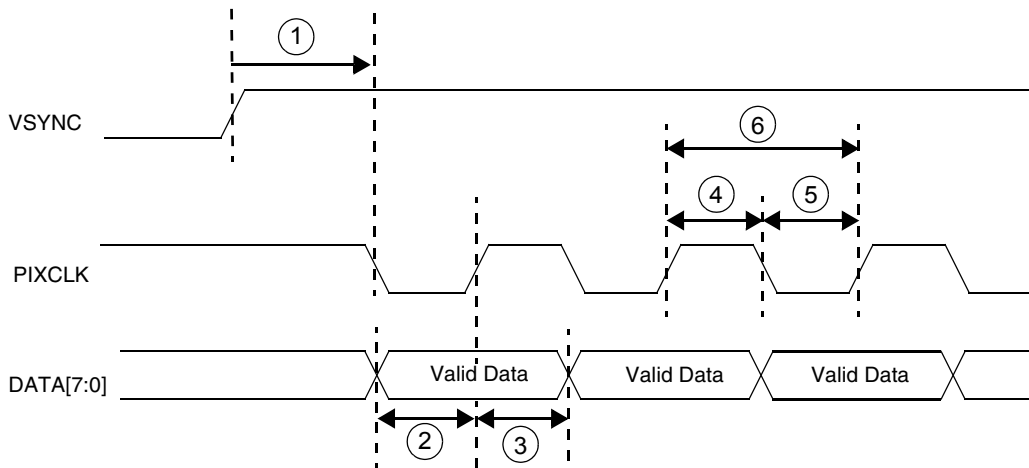
$$\begin{aligned} \text{positive duty cycle} &= 10 / 2 = 5\text{ns} \\ \Rightarrow \text{max rise time allowed} &= 5 - 1 = 4\text{ns} \\ \text{negative duty cycle} &= 10 / 2 = 5\text{ns} \\ \Rightarrow \text{max fall time allowed} &= 5 - 1 = 4\text{ns} \end{aligned}$$

Falling-edge latch data

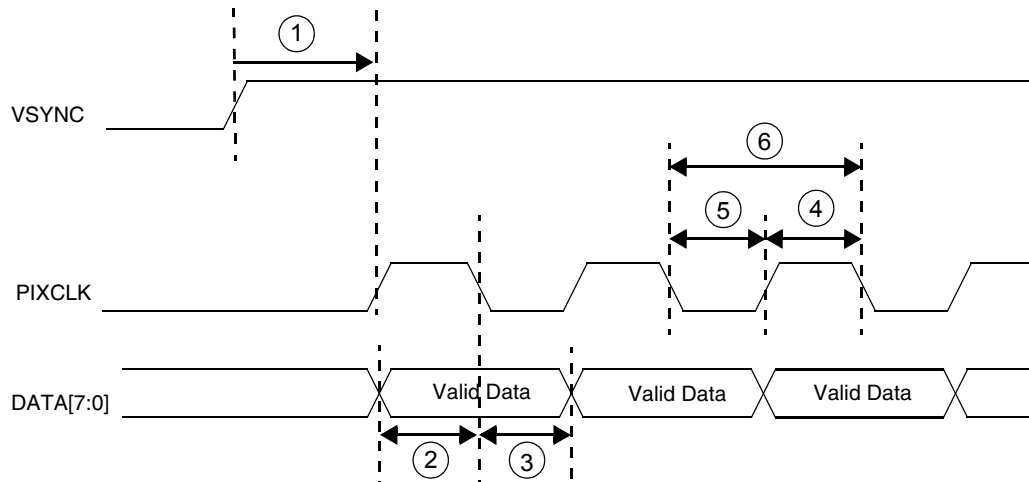
$$\begin{aligned} \text{max fall time allowed} &= (\text{negative duty cycle} - \text{hold time}) \\ \text{max rise time allowed} &= (\text{positive duty cycle} - \text{setup time}) \end{aligned}$$

4.14.2 Non-Gated Clock Mode

Figure 65 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 66 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 35.



**Figure 65. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 66. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 35. Non-Gated Clock Mode Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_pixclk	180	–	ns
2	csi_d setup time	1	–	ns
3	csi_d hold time	1	–	ns
4	csi_pixclk high time	10.42	–	ns
5	csi_pixclk low time	10.42	–	ns
6	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Functional Description and Application Information

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns
negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

5 Pin-Out and Package Information

Table 36 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing table in the reference manual.

Table 36. i.MXL 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS1	SD_DAT3	SD_CLK	NVSS4	USBD_AFE	NVDD4	NVSS3	$\overline{\text{UART1_RTS}}$	UART1_RXD	NVDD3	N.C.	N.C.	QVDD4	N.C.	N.C.	N.C.	A
B	A24	SD_DAT1	SD_CMD	PB16	$\overline{\text{USBD_ROE}}$	USBD_VP	SSL_RXCLK	SSL_TXCLK	SPI1_SCLK	N.C.	N.C.	N.C.	QVSS4	N.C.	N.C.	N.C.	B
C	A23	D31	SD_DAT0	PB15	USBD_RCV	$\overline{\text{UART2_CTS}}$	UART2_RXD	SSL_RXFS	UART1_TXD	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	C
D	A22	D30	D29	PB14	USBD_SUSPND	USBD_VPO	USBD_VMO	SSL_RXDAT	$\overline{\text{SPI1_SPI_RDY}}$	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	$\overline{\text{UART2_RTS}}$	SSL_TXDAT	SPI1_SS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	E
F	A18	D27	D25	A19	A16	PB18	UART2_TXD	SSL_TXFS	SPI1_MISO	N.C.	N.C.	REV	N.C.	N.C.	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	PB17	PB19	$\overline{\text{UART1_CTS}}$	SPI1_MOSI	N.C.	CLS	CONTRAST	ACD/OE	LP/HSYNC	FLM/VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS1	QVSS1	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS1	NVDD1	NVSS2	NVSS2	LD6	LD7	LD8	LD11	QVDD3	QVSS3	J
K	A10	D16	A9	D17	NVDD1	NVSS1	NVSS1	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS1	$\overline{\text{CAS}}$	TCK	TIN	PWMO	CSL_MCLK	CSL_D0	CSL_D1	CSL_D2	CSL_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS1	$\overline{\text{RW}}$	MA10	$\overline{\text{RAS}}$	$\overline{\text{RESET_IN}}$	BIG_ENDIAN	CSL_D4	CSL_HSYNC	CSL_VSYNC	CSL_D6	CSL_D5	M
N	A4	$\overline{\text{EB1}}$	D10	D7	A0	D4	PA17	D1	DQM1	$\overline{\text{RESET_SF}}$	$\overline{\text{RESET_OUT}}$	BOOT2	CSL_PIXCLK	CSL_D7	TMS	TDI	N
P	A3	D9	$\overline{\text{EB0}}$	$\overline{\text{CS3}}$	D6	$\overline{\text{ECB}}$	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	$\overline{\text{TRST}}$	I2C_SCL	I2C_SDA	XTAL32K	P
R	$\overline{\text{EB2}}$	$\overline{\text{EB3}}$	A1	$\overline{\text{CS4}}$	D8	D5	$\overline{\text{LBA}}$	BCLK ¹	D0	DQM0	SDCKE0	POR	BOOT1	$\overline{\text{TDO}}$	QVDD2	EXTAL32K	R
T	NVSS1	A2	$\overline{\text{OE}}$	$\overline{\text{CS5}}$	$\overline{\text{CS2}}$	$\overline{\text{CS1}}$	$\overline{\text{CS0}}$	MA11	DQM2	$\overline{\text{SDWE}}$	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS2	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

¹ burst clock

Table 37 illustrates the package pin assignments for the 225-contact MAPBGA package. For a complete listing of signals, see the Signal Multiplexing table in the reference manual.

Table 37. i.MXL 225 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	SD_CMD	PB15	PB19	$\overline{\text{USBDR}}_{\text{ROE}}$	USBDR_SUSPND	USBDR_VM	SSI_RXFS	SSI_TXCLK	SPI1_SPI_RDY	SPI1_SCLK	REV	PS	LD2	LD4	LD5
B	SD_DAT3	SD_CLK	PB16	USBDR_AFE	USBDR_RCV	USBDR_VMO	SSI_RXDAT	$\overline{\text{UART1}}_{\text{TXD}}$	SPI1_SS	LSCLK	SPL_SPR	LD0	LD3	LD6	LD7
C	D31	SD_DAT0	PB14	PB18	SD_DAT2	USBDR_VPO	UART2_RXD	SSI_TXFS	$\overline{\text{UART1}}_{\text{RTS}}$	CONTRAST	FLM/VSYNC	LD8	LD9	LD12	NVDD2
D	A23	A24	SD_DAT1	PB17	NVDD1	USBDR_VP	QVDD4	UART2_TXD	NVDD3	SPI1_MOSI	LP/HSYNC	LD1	LD11	TMR2OUT	LD13
E	A21	A22	D30	D29	NVDD1	QVSS	$\overline{\text{UART2}}_{\text{RTS}}$	UART1_RXD	$\overline{\text{UART1}}_{\text{CTS}}$	SPI1_MISO	ACD/OE_ACD	LD10	TIN	CSI_D0	CSI_MCLK
F	A20	A19	D28	D27	NVDD1	NVDD1	$\overline{\text{UART2}}_{\text{CTS}}$	SSI_RXCLK	SSI_TXDAT	CLS	QVDD3	LD14	LD15	CSI_D2	CSI_D4
G	A17	A18	D26	D25	NVDD1	NVSS	NVDD4	NVSS	NVSS	QVSS	PWMO	CSI_D3	CSI_D7	CSI_HSYNC	CSI_D5
H	A15	A16	D23	D24	D22	NVSS	NVSS	NVSS	NVSS	NVDD2	CSI_D1	CSI_VSYNC	CSI_PIXCLK	I2C_SDA	TMS
J	A14	A12	D21	D20	NVDD1	NVSS	NVSS	QVDD1	NVSS	CSI_D6	I2C_SCL	TCK	$\overline{\text{TDO}}$	BOOT1	BOOT0
K	A13	A11	$\overline{\text{CS2}}$	D19	NVDD1	NVSS	QVSS	NVDD1	NVSS	D1	BOOT2	TDI	BIG_ENDIAN	$\overline{\text{RESET}}_{\text{OUT}}$	XTAL32K
L	A10	A9	D17	D18	NVDD1	NVDD1	$\overline{\text{CS5}}$	D2	$\overline{\text{ECB}}$	NVSS	NVSS	POR	QVSS	XTAL16M	EXTAL32K
M	D16	D15	D13	D10	$\overline{\text{EB3}}$	NVDD1	$\overline{\text{CS4}}$	$\overline{\text{CS1}}$	BCLK ¹	$\overline{\text{RW}}$	NVSS	BOOT3	QVDD2	$\overline{\text{RESET}}_{\text{IN}}$	EXTAL16M
N	A8	A7	D12	$\overline{\text{EB0}}$	D9	D8	$\overline{\text{CS3}}$	$\overline{\text{CS0}}$	PA17	D0	DQM2	DQM0	SDCKE0	TRISTATE	$\overline{\text{TRST}}$
P	D14	A5	A4	A3	A2	A1	D6	D5	MA10	MA11	DQM1	$\overline{\text{RAS}}$	SDCKE1	CLKO	$\overline{\text{RESET}}_{\text{SF}}$
R	A6	D11	$\overline{\text{EB1}}$	$\overline{\text{EB2}}$	$\overline{\text{OE}}$	D7	A0	SDCLK	D4	$\overline{\text{LBA}}$	D3	DQM3	$\overline{\text{CAS}}$	$\overline{\text{SDWE}}$	AVDD1

¹ Burst Clock

5.1 MAPBGA 256 Package Dimensions

Figure 67 illustrates the 256 MAPBGA 14 mm × 14 mm × 1.30 mm package, with an 0.8 mm pad pitch. The device designator for the MAPBGA package is VH.

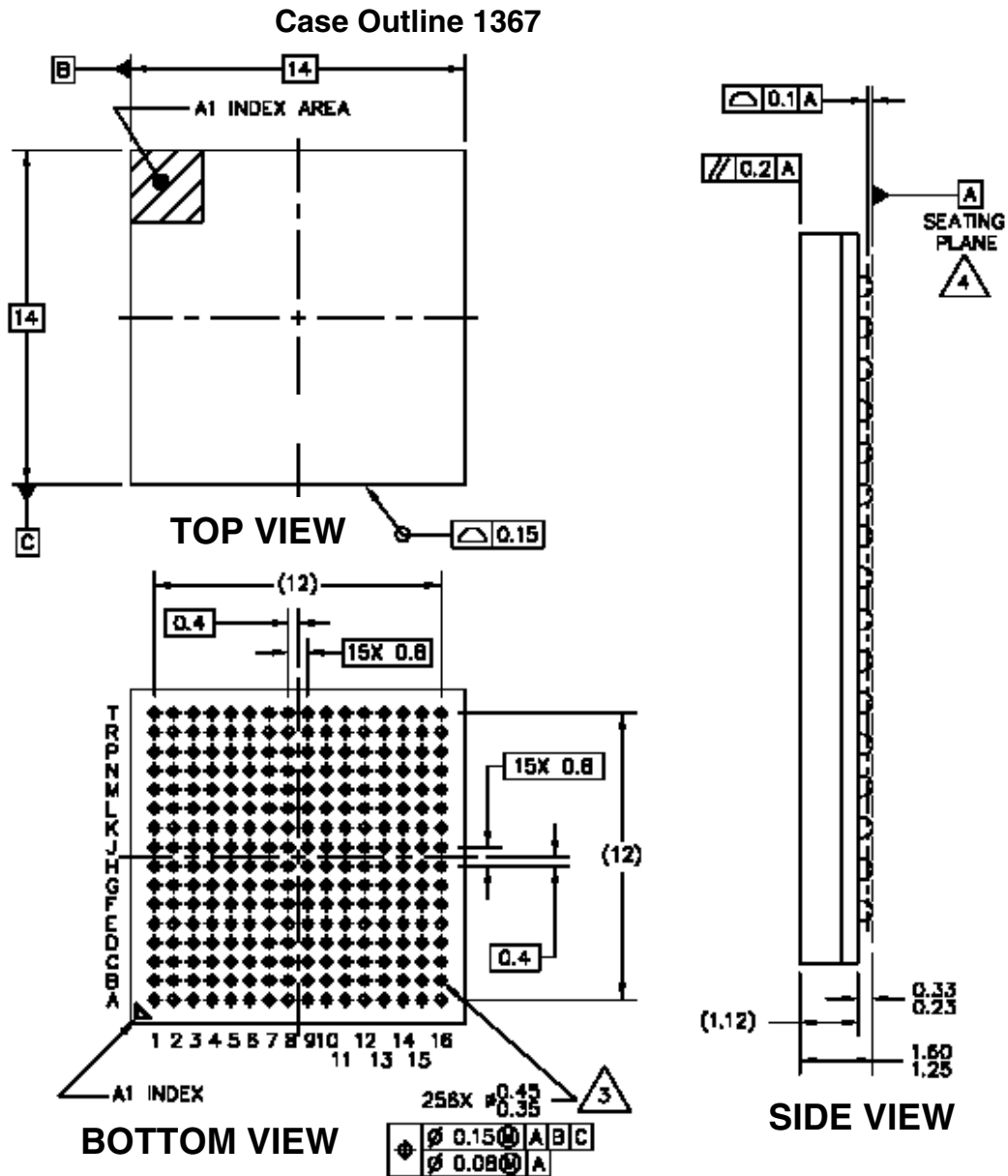
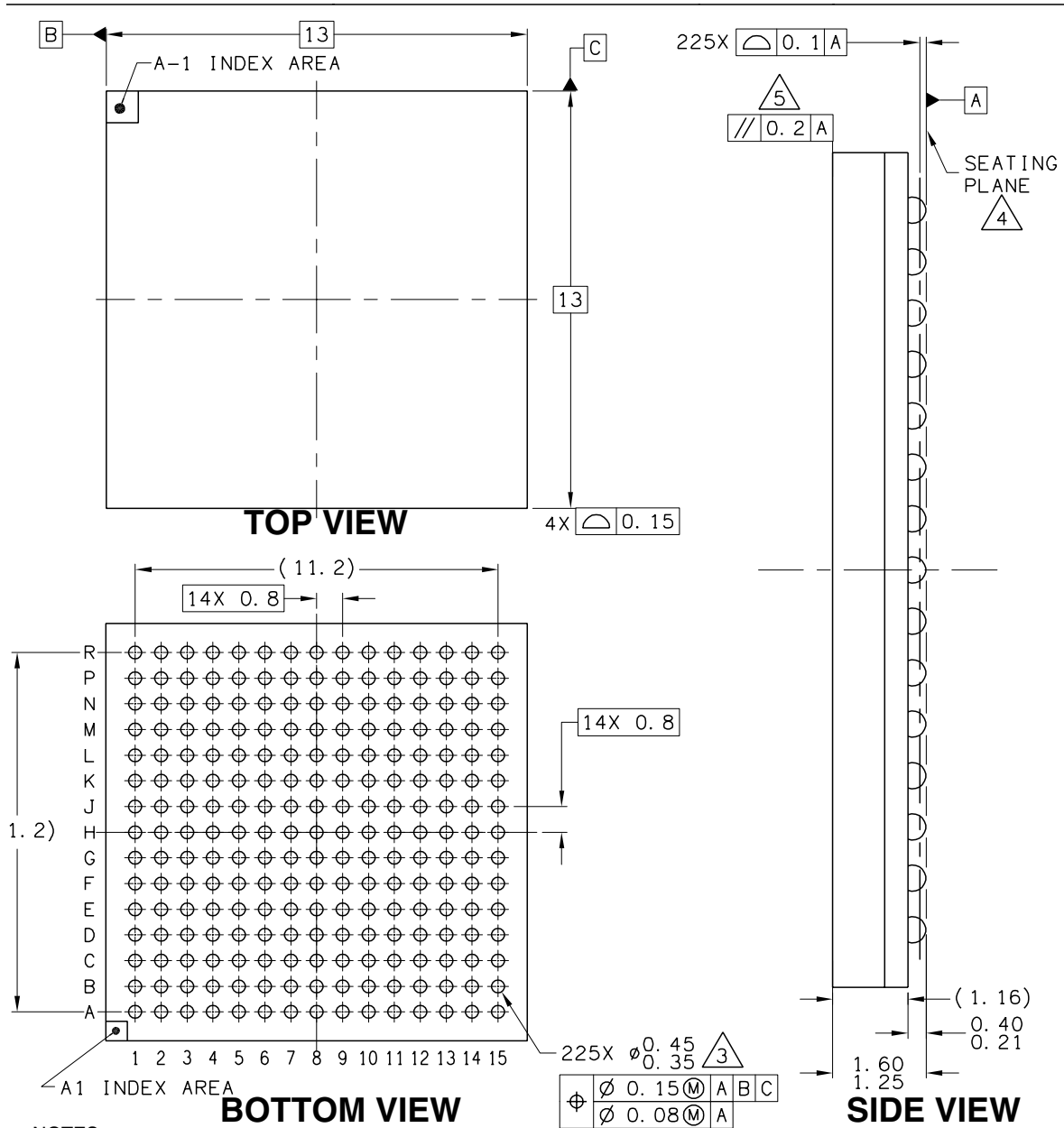


Figure 67. i.MXL 256 MAPBGA Mechanical Drawing

5.2 MAPBGA 225 Package Dimensions

Figure 68 illustrates the 225 MAPBGA 13 mm × 13 mm package.

Case Outline 1304B



NOTES:

- 1 ALL DIMENSIONS ARE IN MILLIMETERS.
- 2 DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
- 3 MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4 DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 68. i.MXL 225 MAPBGA Mechanical Drawing

6 Product Documentation

6.1 Revision History

Table 38 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 38. i.MXL Data Sheet Revision History Rev. 6

Revision
1. Minor technical corrections throughout document. 2. Removed DTACK SEL=0 3. Removed lead package devices. 4. Corrected voltage specifications for SDRAM from 3.3V to 3.0V. 5. Clarified BCLK signal nomenclature. 6. Updated EIM and DTACK timing diagrams. 7. 1.8 +/- 0.1 V columns removed from USB, SPI, and LCD timing parameter tables.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at <http://www.freescale.com/imx>. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from <http://www.arm.com>.

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