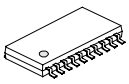
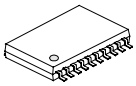
SC73C0302

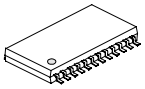
4-BIT MICROCONTROLLER
FOR REMOTE CONTROLLER



SOP-20-300-1.27



SOP-20-375-1.27



SOP-24-375-1.27

DESCRIPTIONS

SC73C0302 is one of Silan's 4-bit CMOS single-chip micro-controllers for infrared remote control transmitters(IRCTs). It can be implemented in various IRCTs circuits by mask option.

SC73C0302 is available in a small plastic shrink SOP package (SOP-20-300-1.27or SOP-20-375-1.27 or SOP-24-375-1.27).

FEATURES

* Operating voltage range: (2.0 ~ 4.0V)
  low static power consumption (<1uA);
* Program memory: 2k x 9bits;
  The last 1k areas also can be used as data table;
* Data memory (RAM):16 x 4bits;
* Timer/counter from 10~15;
* 16 I/O port, one 4-bit input port, one 4-bit output port and two programmable I/O port;
* Oscillator frequency (fosc): 300KHz~2MHz;
* Carrier frequency (fosc/12), 1/3duty (the carrier frequency is 38kHz at fosc=455KHz);
* Cycle of clock:11μs (when operating at fosc=455KHz);
* Handles various user's codes, repeat key, persist-key press and many other functions.

ORDERING INFORMATION

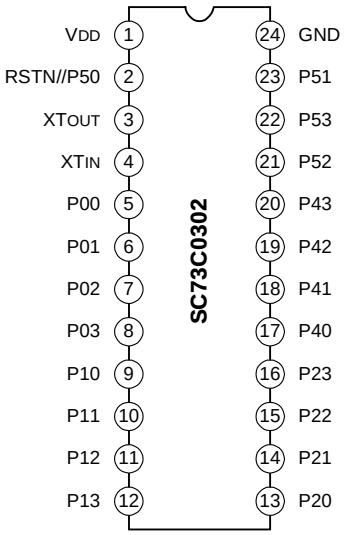
Device	Package
SC73C0302	SOP-24-375-1.27
SC73C0302A	SOP-20-375-1.27
SC73C0302B	SOP-20-300-1.27

APPLICATION

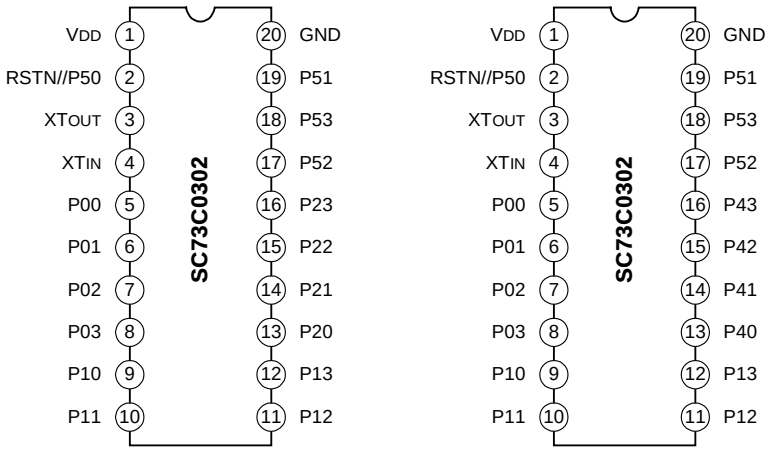
* Infared remote control device such as TV, Video Cassette Recoder, VTR, laser phonograph and acoustics remote controllers.

PIN CONFIGURATIONS

(1). SOP-24

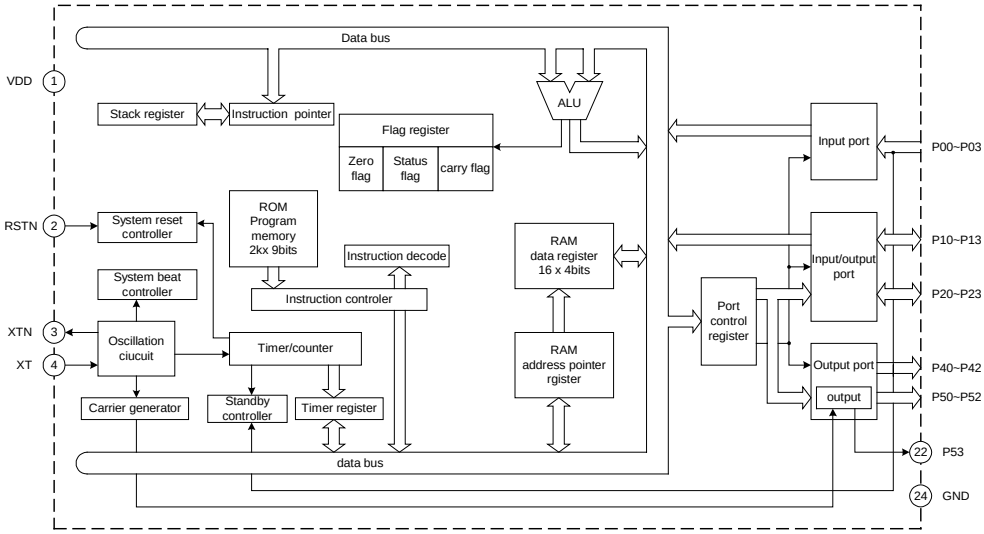


(2). SOP-20



NOTE: Pin 2 can usually be used as the RSTN pin, when there are needs for more pins, this pin can be used as Pin P50.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristics	Symbol	Value	Units
Supply Voltage	V_{DD}	-0.3 ~ +5.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Output Voltage	I_{OUT}(P53)	-20	mA
Power Consumption	P_D	300	mW
Storage Temperature	Tstg	-40~+125	°C
Operating Temperature	Topr	-10~+70	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, V_{DD}=3.0V)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units.
Power Supply Voltage	V_{DD}	All function	2	--	4	V
Operating Voltage	I_{DD}	fosc=455kHz	--	--	1	mA
Oscillation Frequency	F_{OSC}	--	300k	455k	2M	Hz
Static Power consumption	I_{DS}	Oscillator stop	--	--	1	μA
Input pull-down resistor	R	V_{DD}=3V	100	200	400	KΩ
High Input Voltage	V_{IH}	--	0.7V_{DD}	--	V_{DD}	V
Low Input Voltage	V_{IL}	--	0	--	0.3V_{DD}	V
High Output Current	I_{OH}	V_{OH}=1.5V	-10	--	--	mA
Low Output Current	I_{OL}	V_{OL}=1.5V	5	--	--	mA

PIN DESCRIPTION

Pin NO	Symbol	Description
1	VDD	Power supply (2.0V~4.0V)
24	GND	
2	RSTN	Reset （active low）
	P50	P channel open-drain output
3	XTOUT	Crystal oscillator output
4	XTIN	Crystal oscillator input
5~8	P00~P03	4-bit input pin (with internal pull-down resistor). This pin is used for keyboard scan and to control internal circuit.
9~12	P10~P13	4-bit I/O port (It can be set to input or output by program, with internal pull-down resistor). In input mode, it can be used for keyboard scan. In output mode, push-pull output, used for keyboard scan output.
13~16	P20~P23	4-bit I/O port (It can be set to input or output by program, with internal pull-down resistor). In input mode, it can be used for keyboard scan. In output mode, push-pull output, can be used for keyboard scan output.
17~20	P40~P43	4-bit output pin, can be used for keyboard scan output.
21	P52	Large current output (can be used to drive LED), as the denote of it is transmitting signal.
22	P53	Outputs remote signal with carrier.
23	P51	P channel open-drain output.

FUNCTION DESCRIPTIONS

1. PC: 10 bits

PC refers to program counter. The maximum addressing area is 2K bytes in ROM. The program counter contains the address of the instruction that will be executed next. When reset, the value of the PC is cleared to 0. The PC is set to predefined value when one of the 3 following occasions occurs: 1) when the JUMP instruction is executed; 2) when a subroutine call is back; 3) when a program call is back. In the SC73C0302, all instructions is 1-byte OP Code instructions, PC increments by 1 each time an instruction is executed.

2. MBR

Memory buffer register (MBR) is the written-only, higher 4-bit of the program pointer. The ROM of the SC73C0302 can be divided into 16 blocks, each block has 128 bytes. These block can be addressed by the MBR. When the program starts executing a branch instruction, it will load the corresponding value to the MBR register, then executes the command BSS label.

3. STACK

STACK refers to stack register(11 bits). It stores the previous value of program pointer during execution of subroutine calls, 11 bits. Because there is only one-level hardware stack register, only one-level programs can be called. When the user tries to make a nested two-level program call, an error will occur.

4. B, H, D

BHD refers to the pointers to data table. They are 3bit, 4-bit (only the lower 3 bit is valid) and 4-bit. The last 1K byte area of ROM (400H~7FFH) can also be used for data table. When addressing the data of the program in ROM, the registers act as the pointers to the data table. In other cases, the H, D registers can be used as general purpose registers. Data stored in the data table can be addressed by the REF instruction. When executing the REF instruction, the program searches the data in the data table automatically. The lower 10-bit of the ROM is decided by the lower 3-bit of the B register, lower 3-bit of the H register and all bits of the D register.

5. ROM

Address	2k x 9bits
000H	Reset address
001H	
002H ⋮ 01FH	Subroutine address
020H ⋮ 3FFH	Program address
400H ⋮ 7FFH	Data table and program multiplex areas

6. LR

LR refers to the L register (4 bits). It is often used to store the pointer to RAM addresses, and can also be used as a general purpose register.

7. RAM

RAM refers to data memory. It consists of 16 x 4bits and is used to store temporary data and results after a program is executed. There are two RAM addressing modes: one for indirect addressing by the LR register, it can address the entire RAM areas. The other is instruction direct addressing, the lower 3-bit of the instruction specifying the address of the RAM. It can be used to address the lower 8-bit of the RAM, but SC73C0302 does not support this mode. When reset, the contents of RAM are not defined, we recommend users to initialize it at the beginning of the program.

8. ALU

The arithmetic and logic unit plays a leading role in performing various operations of 4-bit binaries. The operation of the ALU will change the carry flag and the zero flag.

9. Acc

4-bit accumulator, it is mostly used to store data and results.

10. CF

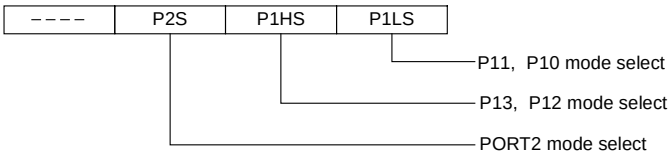
CF refers to carry flag.

11. SF

SF refers to the status flag. When reset, the status flag is set to 1.

12.PR

PR refers to the port register, which specifies the input mode or output mode of the I/O ports, is 4-bit write-only. When PR=1, the corresponding port is set to output mode; PR=0, input mode. The execution of the HOLD instruction won't affect the status of PORT1 and PORT2. When reset, the value of the PR is 0000B.



13. PORT

SC73C0302 has five groups of I/O ports, altogether 20 pins.

P0 port:P03~P00, 4-bit input port, with internal pull-down resistor, it can release the HOLD mode at high level.

P1 port (P13~P10) and P2 port (P23~P20) can be set to input/output mode by program. In input mode, it can release HOLD mode at high level.

P0 port (03, 52, 51, 50) output port.

P5 port (P53, P52, P51, P50)

P50: keyboard scan output pin, push-pull output.

P51: P-channel open drain output, this pin always is used to select system code.

P52: Large current output port, this pin can be used to drive LED display.

P53: Large current output port, this pin can be used to output infrared remote signal. If P53 is set to 1.this pin outputs modulated signal with carrier whose frequency is OSC/12 (1/3 duty). If it is set to 0, this pin outputs low level signal.

When the MCU reads the P5 port, it reads the contents of the timer instead of port status.

P53	P52	P51	P50
IT3	IT2	IT1	IT0

14. Timer/counter

SC73C0302 has a on-chip 17-bit timer. The clock source of the timer is the oscillator frequency (FC) of the circuit. There are timing steps from 10 steps (which generates pulses with frequency $FC/2^{10}$) to 15 ($FC/2^{15}$). The timer outputs pulse frequency ranging from $FC/2^{10}$ to $FC/2^{15}$, can be used for timer after releasing the HOLD mode, can also be used as a WDT. After release the HOLD mode released and the timer reset instruction TMRST executed, the timer value is cleared.

15. TR

TR refers to the timer register. It selects the status of the timer mode, 4-bit write-only. The SC73C0302 has no special instructions to read the register, so please use the following instructions: LD A, %5 or LD @LR, %5。The corresponding relationships are: P53—IT3；P52—IT2；P51—IT1；P50—IT0。

3	2	1	0
IBNS	TIBS		

TR timer register

16. IBNS

The control bit of the read timer. When the value is 0, read P53(IT3), IT2~IT0 become 0; when the value is 1, read 4-bit data 53~P50 (IT3~IT0).

P53: 2^{15}/fosc

P52: 2^{14}/fosc

P51: 2^{13}/fosc

P50: 2^{12}/fosc

TIBS: only valid when IBNS=0

000: 2^{10}/fosc	50% duty	100: 2^{12}/fosc	75% duty
001: 2^{11}/fosc	50% duty	101: 2^{13}/fosc	50% duty
010: 2^{11}/fosc	75% duty	110: 2^{13}/fosc	75% duty
011: 2^{12}/fosc	50% duty	111: 2^{14}/fosc	50% duty

The value of timer increments by 1 each time a clock is coming. When executing the instruction IN %5, A=LD A, %5 and IN %5, @LR=LD @LR, %5, the timer sends the complement value of the counter to the A and RAM. Therefore, after reset, every bit of the read timer is set to 1.

The maximum adjustable time of the timer is 2^{16}/FC. When the timer acts as a WDT and the timer is activated, it must execute the TMRST instruction and clear the timer in 2^{16}/FC's time, otherwise, it will lead the WDT to overflow, and cause the MCU to reset.

INSTRUCTION SETS

1.Transmit instruction:

Instruction	Operation	CF	SF	Cycle
LD A, L	A ← LR	---	1	1
LD A, D	A ← DC	---	1	1
LD A,H	A ←HR	---	1	1
LD A, @LR	A ← RAM(LR)	---	1	1
LD A, #k	A ← k	---	1	1
LDL A, @HD	A ← ROM(HD)L	---	1	2
LDH A, @HD	A ← ROM(HD)H	---	1	2
LD L, A	LR ← A	---	1	1
LD L, #k	LR ← k	---	1	1
LD @LR, A	RAM(LR) ← A	---	1	1
LD @LR, #k	RAM(LR) ← k	---	1	1
LD DC, A	DC ← A	---	1	1
LD P, A	PR ← A	---	1	1
LD T, A	TR ← A	---	1	1
LD B, A	BR ← A	---	1	1
LD H, A	HR ← A	---	1	1

a. LD A, L Load values in the LR register to the accumulator.
b. LD A, D Load values in the DC register to the accumulator.
c. LD A, H Load the values in the HR register to the accumulator.
d. LD A, @LR Load the contents of RAM pointed at by the LR register to the accumulator.
e. LD A, #k Load the 4-bit immediate K to accumulator.
f. LDL A, @DC Load the lower 4-bit of ROM data pointed at by the HD to the accumulator.
g. LDH A, @HD Load the higher 4-bit of ROM data pointed at by the HD to the accumulator.
h. LD L, A Load the contents of the accumulator to the LR register.
i. LD L,#K Load immediate K to the LR register.
j. LD @LR, A Load the content of the accumulator to RAM pointed at by the LR register.
k. LD @LR, #k Load the immediate K to RAM pointed at by the LR register.
l. LD DC, A Load the content of the accumulator to the DC register.
m. LD P, A Load the content of the accumulator to the port register(PR).
n. LD T, A Load the content of the accumulator to the timer register.
o LD B, A Load the content of the accumulator to the BR register.
p LD H, A Load the content of the accumulator to the HR register.

Executing the above 15 transmit instructions will not affect the carry flag and the status flag remains 1.

2. Input/output instruction

Instruction	Operation	CF	SF	Cycle
IN A, %p	A ← PORT(p)	---	/Z	2
IN @LR, %p	@LR ← PORT(p)	---	/Z	2
OUT %p, A	PORT(p) ← A	---	1	2
OUT %p, @LR	PORT(p) ← @LR	---	1	2

a. IN A, %P Move the value of port(P) to the accumulator

b. IN @LR, %p Move the value of port(P) to ROM pointed at by the LR register.

c. OUT %p, A Move the contents of the accumulator to port (P).

d. OUT %p, @LR Load the contents of RAM pointed at by the LR register to port(P).

The above four input/output instructions are used mostly for port operation, the two read instructions will affect the status flag SF.

3. Arithmetic and logical instructions

Instruction	Operation	CF	SF	Cycle
ADD A, @LR	A ← A+RAM (LR)	---	/C	1
ADDC A, @LR	A ← A+RAM (LR)+CF	C	/C	1
ADD A, #k	A ← A+k	---	/C	1
ADD L, #k	LR ← LR+k	---	/C	2
SUBRC A, @LR	A ← RAM(LR)-A-/CF	C	C	1
INC @LR	RAM(LR) ← RAM(LR)+1	---	/C	1
DEC @LR	RAM(LR) ← RAM(LR)-1	---	C	1
INC D	DC ← DC+1	---	/C	1
DEC D	DC ← DC-1	---	C	1
AND A, @LR	A ← A&RAM(LR)	---	/Z	1
OR A, @LR	A ← A | RAM(LR)	---	/Z	1
XOR A, @LR	A ← A^RAM(LR)	---	/Z	1

a. ADD A, @LR Add the contents of RAM pointed at by the LR to accumulator. Store the sum in the ACC. This operation will affect SF, SF=/CF.

b. ADDC A, @LR Add the contents of RAM pointed at by the LR register to accumulator with carry. Store the carry bit in the CF. This operation will affect SF, SF=/CF.

c. ADD A, #K Add immediate K to accumulator. Store the sum in the ACC. This operation will affect SF, SF=/CF.

d. ADD L, #K Add immediate K to the LR register. Store the sum in the LR. This operation will affect SF, SF=/CF.

e. SUBRC A, @LR Subtract instruction with borrow(the complement of carry). Subtract the contents of the accumulator from the contents of RAM pointed at by the LR register, subtract the complement of the carry bit, then store the results in the accumulator, transfer the carry bit to the CF. This will affect SF and CF, SF=CF.

f. INC @LR — Increment instruction, it increments the contents of RAM pointed at by the LR register by 1. This will affect SF, SF=/CF.

g. DEC @LR — Decrement instruction. The contents of RAM pointed at by the LR register decrement by 1. This will affect SF, SF=CF.

h. INC D — Increment instruction, it increments the contents of the D register by 1. This will affect SF, SF=/CF.

i. DEC D — Decrement instruction, it decrements the contents of the D register by 1. This will affect SF, SF=/CF.

j. AND A, @LR — The contents of the accumulator and RAM pointed at by the L register are ANDed and the results are stored in the accumulator. SF changed, SF=/Z.

k. OR A, @LR — The accumulator content and the contents of RAM pointed at by the L register are ORed and the results are entered in the accumulator. SF changed, SF=/Z.

l. XOR A, @LR — The contents of the accumulator and RAM pointed at by the L register are XORed and the results are stored in the accumulator. SF changed, SF=/Z.

4. Bit operation instructions

Instruction	Operation	CF	SF	Cycle
CLR @LR, b	RAM(LR)b←0	---	1	2
SET @LR, b	RAM(LR)b←1	---	1	2
TEST @LR, b	SF←/RAM(LR)b	---	*	2

a. CLR @LR, b — Clear the B bit of the RAM pointed at by the LR register.

b. SET @ LR, b — Set the B bit of the RAM pointed at by the LR register to be 1.

c. TEST @LR, b — Test the B bit of the RAM pointed at by the LR register. If this bit is1, the SF is set to 0; otherwise , the SF is set to 1.

5. Carry operation instructions

Instruction	Operation	CF	SF	Cycle
CLR CF	CF←0	0	1	2
SET CF	CF←1	1	1	2
TESTP CF	SF←CF	---	*	1

a. CLR CF — Clear the carry flag to logic zero.

b. SET CF — Set the carry flag to logic 1.

c. TESTP CF — Test the carry flag, sent the carry flag to SF.

6. Branch instructions

Instruction	Operation	CF	SF	Cycle
BSS label		---	1	2
LD MBR, #k		---	---	1

Only when SF is 1, the JUMP instruction is executed, otherwise it will execute the next instruction.
Notes:

a. label Jump destination address
b. #k Immediate (0~15)
c. b Bit addressing (0~3)
d. %p Port address

7. Subroutine instructions

Instruction	Operation	CF	SF	Cycle
CALLS label		---	---	2
RET		---	---	2

When executing subroutine call and return instructions, the subroutine starting address is limited from 000H to 01FH。

8. Others

Instruction	Operation	CF	SF	Cycle
HOLD		---	1	1
NOP		---	---	1
TMRST	Reset timer counter	---	---	1

a. HOLD instruction After executing this instruction , the MCU is in the power-save mode, the clock stops oscillation, and power consumption reduces.
b. NOP instruction Null operation. It doesn't affect anything.
c. TMRST Timer clear command, it will clear all values of the timer to 0. This instruction is often used to reset the WDT in program.

Note: C: CF, if a carry occurred when executing addition instructions or a borrow does not occur when executing substrate instructions ,the carry flag is 1.
Z: Zero, when the data sent to ACC and RAM is 0, the zero flag is 1.
*: This flag denotes the value of the flag is directly pointed at by the instruction.
--: Denote don't affect the flag.

MAP OF INSTRUCTION ADDRESS

H5/L4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	AND A,@LR	OR A,@LR	XOR A,@LR	ADD A,@LR	ADDC A,@LR	SUBRC A,@LR	LD A,@LR	HOLD	DEC @LR	INC @LR	DEC D	INC D	LD L,A	LD D,A	LD A,D	LD A,L
01	LDA,#k															
02	LDL,#k															
03	LD@LR,#k															
04	ADDA,#k															
05	*ADDL,#k*															
06	*IN%p,A*						*LDH A,@HD*	*LDL A,@HD*	*IN%p,@LR*						*RET*	
07	*OUTA,%p*						LD @LR,A	TESTP CF	*OUT@LR,%p*						LDP,A	NOP
08	*SET@LR,b*				*CLR@LR,b*				TMRST	*SET CF*	LD T,A	*CLR CF*	*TEST@LR,b*			
09																
0A		*CALLS a*														
0B	LD MBR,#k															
0C									LD H,A	LD A,H	LD B,A					
0D																
0E																
0F																
10	*BSS a*															
11																
12																
13																
14																
15																
16																
17																
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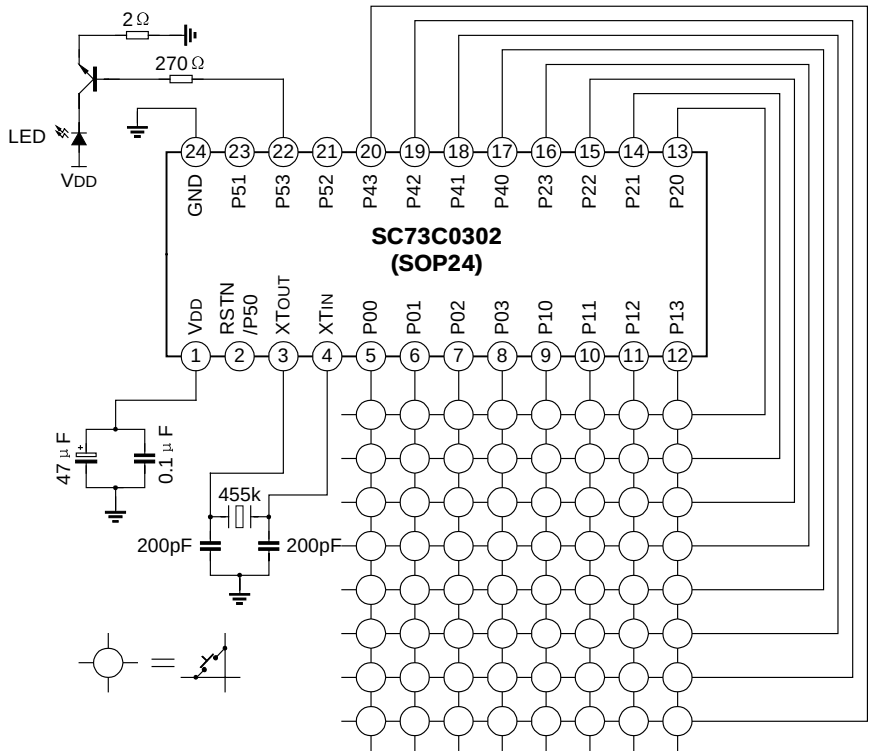
19																
1A																
1B																
1C																
1D																
1E																
1F																

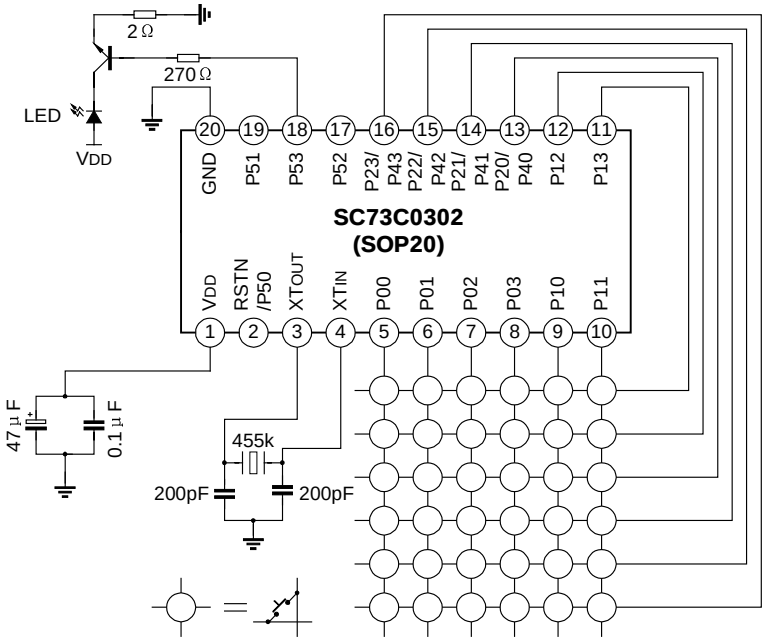
TYPICAL APPLICATION CIRCUIT



Note:1. The connections of the two capacitors with VDD should be as close as possible to the application circuits.

2. The connections between the two capacitors and the VDD, the two capacitors and the ground should be as short as possible.

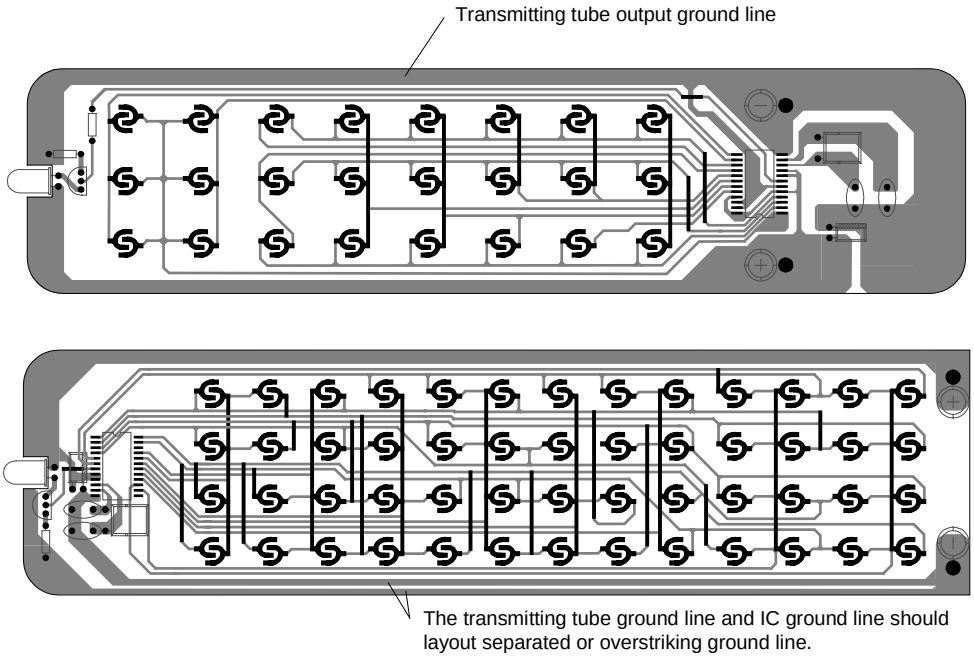
TYPICAL APPLICATION CIRCUIT (continued)



Note:1. The connections of the two capacitors with VDD should be as close as possible to the application circuits.

2. The connections between the two capacitors and the VDD, the two capacitors and the ground should be as short as possible.

PCB WIRE LAYOUT SCHEMATIC:



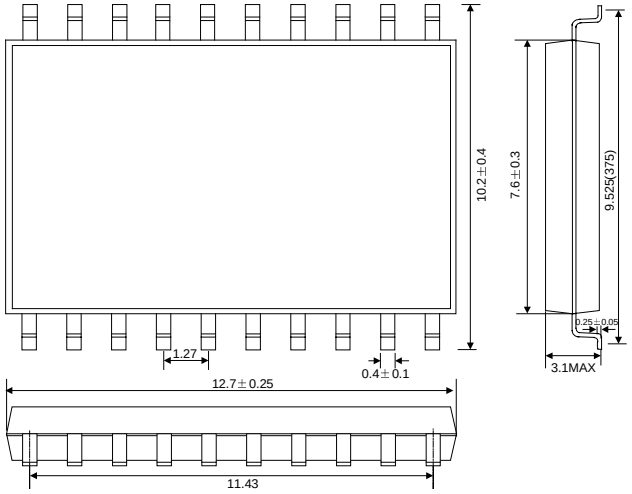
The above IC only use to hint, not to specified.

Note:

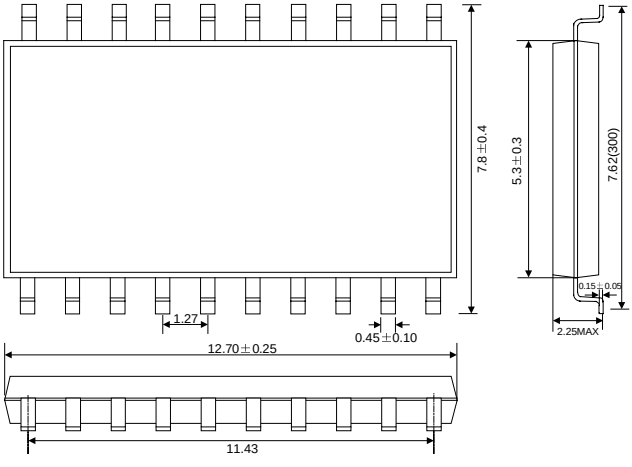
* In wire layout, the power-filter-capacitor should be placed near to the IC.
* In wire layout, the user should avoid long power line and ground line.
* It is recommended infrared transmission unit and the IC ground line be laid out separately, or widening the connection lines.
* The emitter of the triode should connect a 1Ω resistor at least.
* It is recommended to use the 9014 triode.

PACKAGE OUTLINE

SOP-20-375-1.27 Unit: mm

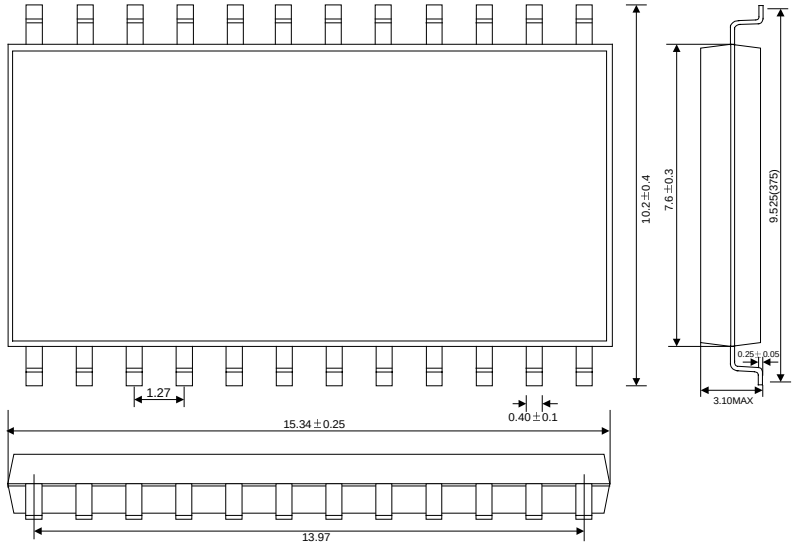


SOP-20-300-1.27 Unit: mm



PACKAGE OUTLINE

SOP-24-375-1.27 Unit: mm



Attach

Revision History

Data	REV	Description	Page
2001.02.20	1.0	Original	
2002.02.26	1.2	Add the “Ordering information”	1
		Modify the “Absolute maximum rating”	3
		Modify the “Typical application circuit “	13-14
		Add the “PCB wire layout schematic”	15
		Modify the “Package outline”	16-17