PO2030N Data sheet (Brief)

Pixelplus Co.,Ltd

PO2030N
1/4.5 Inch VGA Single Chip CMOS IMAGE SENSOR

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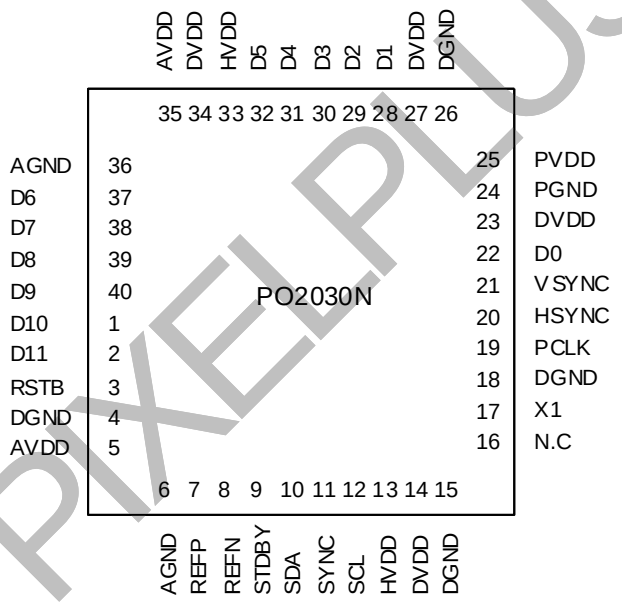
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Features

- 1/4.5 inch 640 X 480 active pixel array with color filters and micro-lens.
- Power supply 2.5V for core and 2.5 ~ 2.8V (Max. 3.1V) for I/O.
- Output formats : 8bit YCbCr / 9Bit Bayer data / 5:6:5 RGB, 12bit 8:8:8 RGB / 8bit Y
- 30 frames/sec progressive scan @27 MHz master clock.
- Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation.
- Still image capture with electrical or mechanical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- VGA / QVGA / QQVGA Scaling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker cancellation.
- Package : 40 pin CLCC, 32 pin CSP



< Figure. 1> Pin Diagram

Table 1. Typical Parameters

Pixel Array	648 X 488
Pixel Size	5.2um X 5.2um
Image Area	3.37mm X 2.54mm
Clock Rate	27 MHz (Max.)
Frame rate	Variable up to 30fps
Dark Current	0.3 nA/㎠
Sensitivity	5V/Lux.sec @15fps,IR cut filter
Saturation Level	770 mV
Conversion Gain	15~50 ㎶/electrons
Fill Factor	40 %
Supply voltage	2.5~2.8V I/O,2.5V Core
Power consumption	32mA @15fps, active HVDD=2.8V,Core=2.5V
	30 uW @standby
Operation Temp.	-30 ~ 40℃
Dynamic Range	68 dB
Package	40 pin CLCC, 32 pin CSP

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PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	D10	O	Bit 10 of data output. Luminance data Y<7:0> are mapped to output pins D<11:4>. Chrominance data UV<7:0> are also mapped to output pins D<11:4>. Bayer RGB data are mapped to output pins D<11:2>.
2	D11	O	Bit 11 of data output.
3	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
4	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
5	AVDD	P	Analog vdd : 2.5V DC. 100nF capacitor to AGND.
6	AGND	P	Analog ground.
7	CREF_P	O	ADC reference voltage. 100nF capacitor to AGND. ADC assumes V(REFP) – V(REFN) is the minimum input voltage that will be converted to 1FFh.
8	CREF_N	O	ADC reference voltage. 100nF capacitor to AGND.
9	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<11:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. MCLK must be fixed to '1' or '0' after STDBY is set to '1' to avoid the leakage current. All registers retain their current values.
10	SDA	I/O	I2C serial data bus.
11	SYNC	O	Mechanical Shutter Close command Output.
12	SCL	I	I2C serial clock input.
13	HVDD	P	Digital vdd for I/O : DC 2.5~3.1V. Voltage range for all output signals is 0V ~ HVDD.
14	DVDD	P	Digital vdd for core logic : 2.5 V DC. 100nF capacitor to DGND.
15	DGND	P	Digital ground for core and I/O circuits.
16	N.C	-	No Connection
17	X1	I	Master clock : Crystal input pad.
18	DGND	P	Digital ground.

Table 2-1. PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
19	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
20	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
21	VSYNC	O	Vertical sync : Indicates the start of a new frame.
22	D0	O	Bit 0 of data output.
23	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
24	PGND	P	Ground for pixel array.
25	PVDD	P	Pixel array current is supplied from PVDD : 2.5V DC. 100nF to AGND
26	DGND	P	Digital ground.
27	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
28	D1	O	Bit 1 of data output.
29	D2	O	Bit 2 of data output.
30	D3	O	Bit 3 of data output.
31	D4	O	Bit 4 of data output.
32	D5	O	Bit 5 of data output.
33	HVDD	P	Vdd for I/O : 2.5~3.1V
34	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
35	AVDD	P	Analog vdd : 2.5V DC, 100nF to AGND
36	AGND	P	Analog ground.
37	D6	O	Bit 6 of data output.
38	D7	O	Bit 7 of data output.
39	D8	O	Bit 8 of data output.
40	D9	O	Bit 9 of data output.

Table 2-2. PIN Description

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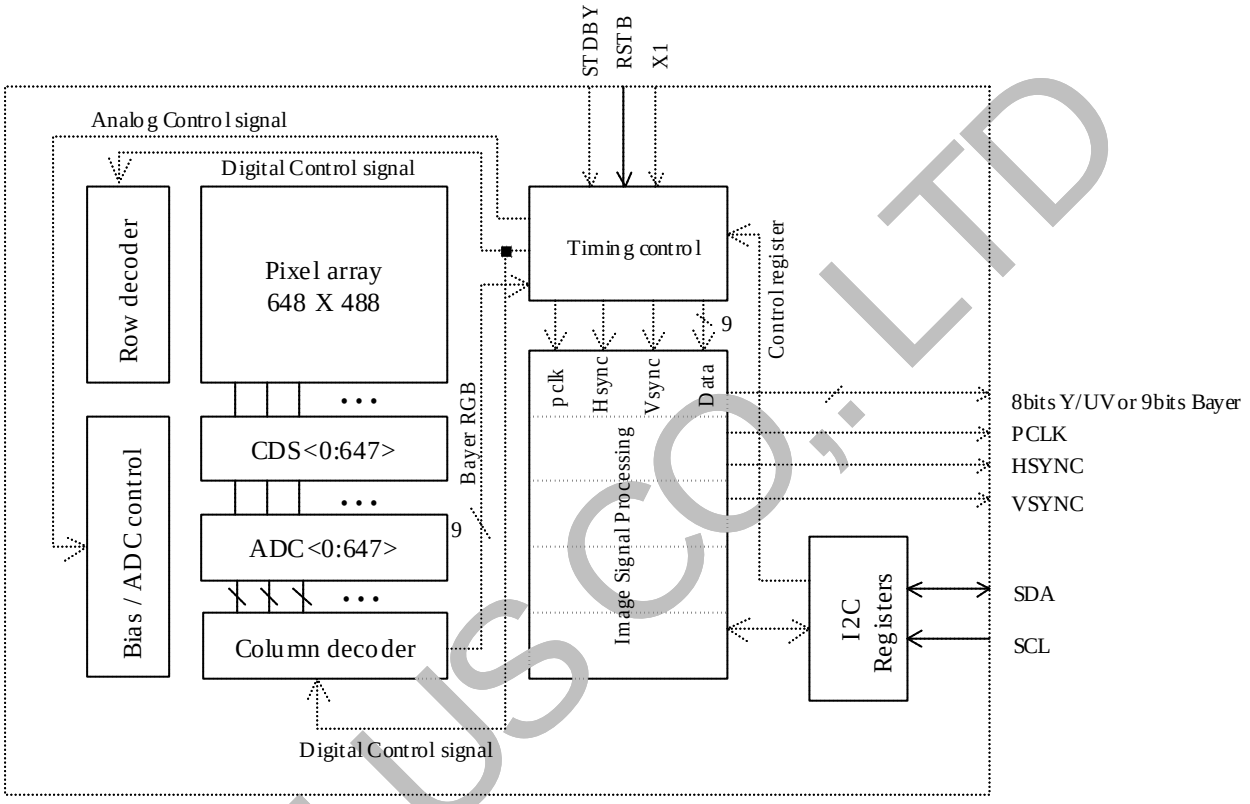
Block Diagram



<Figure. 2> Block Diagram

PO2030N has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through I^2C serial interface.

Electrical Characteristics

Absolute Maximum Ratings*

VDD Supply Voltage ---------- -0.3V to 3.5V
DC Voltage at any input pin ---------- -0.3V to VDD+0.3V
DC current at any input pin ---------- -10mA to +10mA
Storage Temperature ---------- -40?C to +125 ?C

Table 3. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DD}	Digital, Analog, Pixel VDD voltage relative to GND(DGND, AGND, PGND) level.	2.2	2.5	2.8	V
$V_{DD.RECOMMEND}$	Recommended V_{DD} for image quality	2.4	2.5	2.6	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	2.2	2.5 or 2.8	3.1	V
I_{DD1}	Supply current at 15 fps. Currents are programmable through I2C serial interface.		26	32	mA
I_{DD2}	Standby supply current		3	12	uA
V_{IL1}	Input voltage LOW level			0.2*HVDD	V
V_{IH1}	Input voltage HIGH level	0.8*HVDD			V
V_{IL2}	Input voltage LOW level for SCL, SDA.			0.2*HVDD	V
V_{IH2}	Input voltage HIGH level for SCL, SDA.	0.8*HVDD			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1*HVDD	V
V_{OH1}	Output Voltage HIGH	0.9*HVDD			V
V_{OL2}	Output Voltage LOW level for SCL, SDA.			0.2	V
V_{OH2}	Output Voltage HIGH level for SCL, SDA.	HVDD-0.2			V
I_{IN}	Input leakage current		0.005	1	uA
Iot	Output leakage current		0.005	1	uA

(1)Core power is recommended to 2.5V for image quality.
If lower than 2.5V, dynamic range can be decreased
and if higher than 2.5V, the image quality can be degraded due to the color noise.

* Excessive stresses may cause permanent damage to the device.

Table 4. AC Characteristics (All outputs : 15pF load conditions)

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency			27	MHz
duty	Master clock duty cycle	45	50	55	%
t1	Master clock rise/fall time		10		ns
t2	PCLK rise/fall time		15		ns
t3	MCLK falling edge to HSYNC			15	ns
t4	MCLK falling edge to digital output			15	ns
t5	MCLK rising to PCLK			15	ns

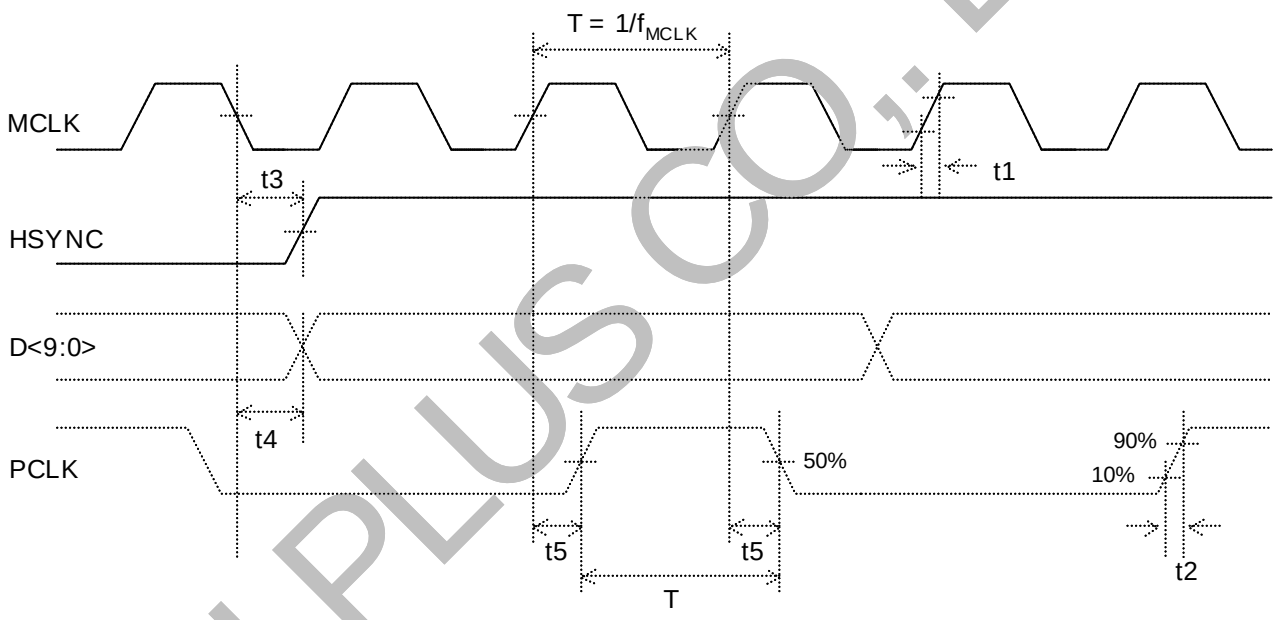


Fig. 13 Clock, Data, and Sync Timing.

Symbol	Descriptions	Min	Typ	Max	Unit
t6	Reset time	8			T

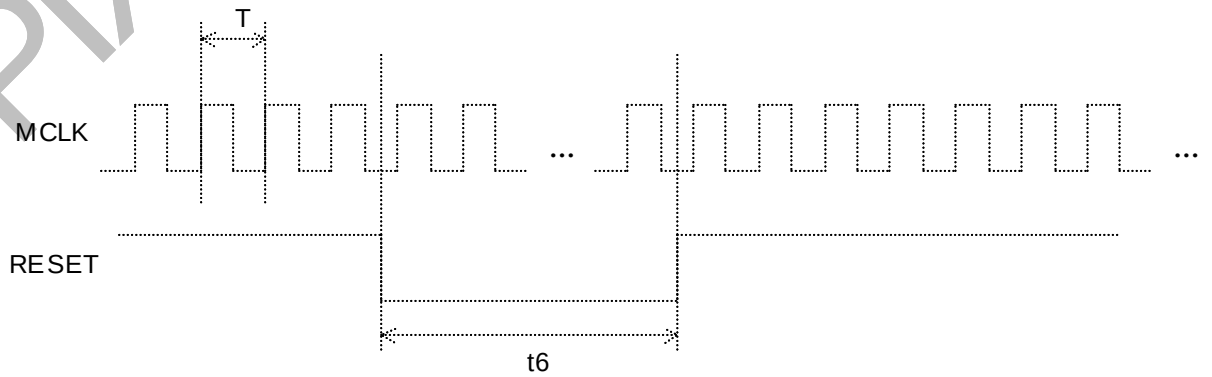


Table 5. Electro- Optical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		5.1		V/Lux.sec
Vsat	Saturation Level	2)		0.77	0.8	V
Vdrk	Dark Signal	3)		0.302		mV
PSNU	PIXEL Signal NON-Uniformity	4)		4	7.5	%
DR	Dynamic range	5)		68		dB

Notes :

1) Measured sensitivity of Green pixel at 1.5lux illumination for 66ms integration time
   Test area is the 128x96 of center area
2) For λ=550 wavelength
3) Measured at the zero illumination for 66ms at the 40 degree
   (1) read the dark signal average of all pixels (640x480) for 66ms
   (2) read the dark signal average of all pixels (640x480) for 0.132ms
   (3) Dark signal @66ms(1)-Dark signal @0.132ms(2)
   (4) convert to mV unit
4) For 16X12 pixel region under illumination with output signal equal to 50% of saturation signal. @128x96 of center area.

$$\frac{\text{Max value of Block} - \text{Min value of Block}}{\text{Average value of all blocks}} \times 100$$

5) For frame rate = 15 fps
   20*Log (Saturation Signal / Dark signal) [dB]

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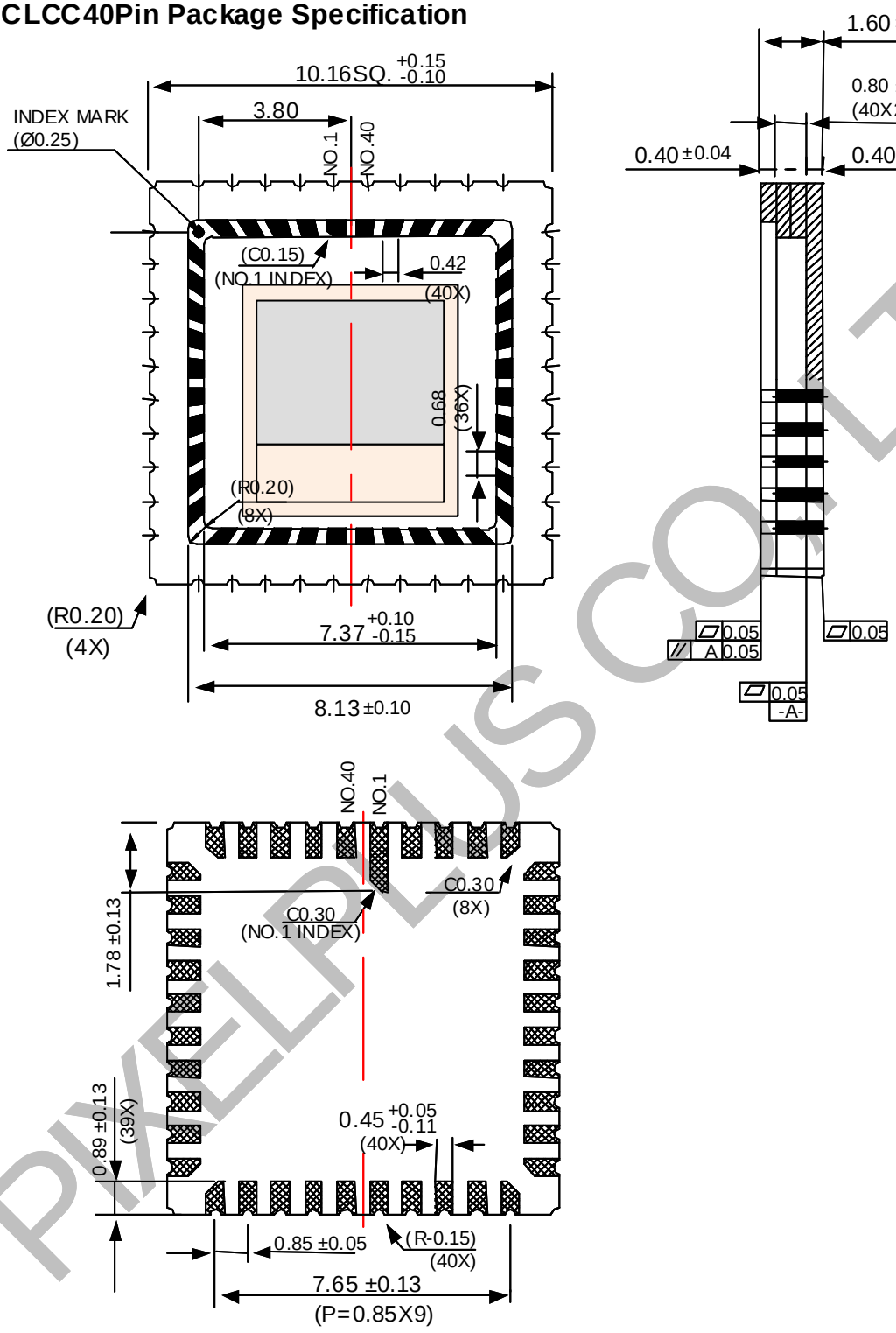
CLCC40Pin Package Specification



NOTE:
1. NI 2.0um + Au 0.5um MIN
2. NO METALLIZATION ON SEAL RING AND DIE ATTACH PAD.
3. UNIT : mm